Test Generation for Acyclic Sequential Circuits with Hold Registers

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Abstract. We present a method of test generation for acyclic sequential circuits with *hold* registers. A *complete (100% fault efficiency)* test sequence for an acyclic sequential circuit can be obtained by applying a *combinational* test generator to all the *maximal time-expansion models (TEMs)* of the circuit. We propose a class of acyclic sequential circuits for which the number of maximal TEMs is one, i.e, the *maximum* TEM exists. For a circuit in the class, test generation can be performed by using only the maximum TEM. The proposed class of sequential circuits with the maximum TEM properly includes several known classes of acyclic sequential circuits such as balanced structures and acyclic sequential circuits without hold registers for which test generation can be also performed by using a combinational test generator. Therefore, in general, the hardware overhead for partial scan based on the proposed structure is smaller than that based on balanced or acyclic sequential structure without hold registers.

Keywords. Acyclic sequential circuits, combinational test generation, hold registers, maximum time-expansion model, partial scan.

1 Introduction

Test generation for sequential circuits is generally considered to be a hard problem. For such sequential circuits, *design for testability (DFT)* is an important approach to reducing the test generation cost [1, 2]. On the other hand, for combinational circuits, efficient test generation algorithms were proposed, and hence we can obtain a *complete (100% fault efficiency)* test set even if the circuit size is large. Therefore, it is significant to apply DFT to a sequential circuit so that the resultant circuit can be test-generated using only a combinational test generator.

Full scan design referring to chaining all of memory elements or flip-flops (FFs) into a shift register is such a traditional DFT technique. In the full scan design, the portion of the circuit excluding the scan path, which is called the *kernel*, is a combinational circuit, and consequently a combinational test generator can be used. However, the full scan design requires large overhead. Although *partial scan design* which makes a subset of FFs scannable can avoid such a penalty, the kernel circuit is still sequential one [3, 4], and hence it requires the use of sequential test generators in general.

In order to obtain *complete test sequences* for sequential circuits efficiently with low hardware overhead, several classes of sequential circuits for which test generation can be performed by using only a combinational test generator were identified [5]–[11]. In [11], we presented a method of test generation for acyclic sequential circuits using a *time-expansion model (TEM)*. One can obtain a *complete* test set for a given acyclic sequential circuit by applying combinational test generation to the TEM of the given circuit, provided that the combinational test generator can deal with multiple faults. Thus, for any sequential circuit, by selecting a sufficient set of scan FFs so that the resultant kernel is acyclic, a *complete test sequence* for the sequential circuit can be generated by using a combinational test generator in spite of partial scan. In [11], however, a *hold register* which is a collection of FFs with a *hold mode* is regarded as a self-loop, and consequently it is always chosen as a scan register.

In this paper, we propose a *new* TEM (time-expansion model) for acyclic sequential circuits with *hold* registers. Even if an acyclic sequential circuit has hold registers, test generation for the circuit can be performed by applying combinational test generation to the new TEM. Hence, hold registers are not necessarily chosen as scan registers, and consequently the hardware overhead is smaller compared with that of the partial scan design in which kernels have no hold register [11].

For an acyclic sequential circuit, a TEM is obtained from a sequence of load/hold controls. Since there exist many sequences of load/hold controls, many TEMs are obtained from an acyclic sequential circuit. Hence, in order to obtain a complete test sequence for an acyclic sequential circuit, we may have to perform test generation for *all* TEMs of the circuit. However, that may not be acceptable. Therefore, in order to reduce the number of TEMs required for the test generation, we introduce a *cover relation* among TEMs for an acyclic sequential circuit, and show that test generation for all *maximal* (on the relation) TEMs is necessary and sufficient to obtain a *complete* test sequence. Furthermore, we present a class of acyclic sequential circuits for which the number of maximal TEMs is just one, i.e., the *maximum*

TEM exists. For a circuit in the class, a test sequence for any testable fault can be generated by using only the maximum TEM of the circuit, and therefore a complete test sequence for the circuit can be obtained efficiently.

2 Time-Expansion Model for Acyclic Sequential Circuits

2.1 Circuit Model

In this paper, we consider synchronous sequential circuits. A sequential circuit consists of combinational logic blocks connected with each other directly or through registers. A register is a collection of D-type flip-flops (FFs) driven by the same clock signal. The clock signals of all registers are assumed to be directly controlled by primary inputs, and no clock signal feeds data input of either a combinational logic block or a register.

A combinational logic block (or logic block, for short) in a sequential circuit is a region of connected combinational logic, excluding registers. A logic block may include primary inputs and primary outputs.

Some registers may have a load enable control signals. A register with an explicit load enable control signal is called *H-register*. An H-register has two modes of operation: a HOLD mode (in which it retains its value across consecutive clock cycles) and a LOAD mode (in which it reads from the data input when a clock signal is applied). A register without a load enable control signal is called *L-register*, which always operates in the load mode during every clock cycle. The control signal for each H-register is assumed to be directly controlled by a primary input independent of that for the others.

An input-pattern for a sequential circuit consists of a data input-pattern and a control input-pattern, which are a collection of signals applied to combinational logics and that of signals applied to H-registers, respectively.

Under this constraint, the topology of a sequential circuit can be modeled by a *topology graph* defined as follows.

Definition 1 (Topology graph): A topology graph is a directed graph $G = (V, A, r)$, where a vertex $v \in V$ denotes a logic block and an arc $(u, v) \in A$ denotes a connection from u to v and each arc has a label $r : A \to \mathcal{Z}^+$ (non-negative integers) $\cup \{h\}$. When two logic blocks u, v are connected directly or through one or more L-registers, the label $r(u, v)$ denotes the number of L-registers (i.e., $r(u, v) \in \mathcal{Z}^+$). When two logic blocks u, v are connected through one H-register [1], the label $r(u, v) = h$. □

[1]Even if there exist two H-registers or both of L and H-registers between two logic blocks, the topology graph can also represent such sequential circuits by supposing existence of a combinational logic block consisting only of lines or buffers between the two logic blocks.

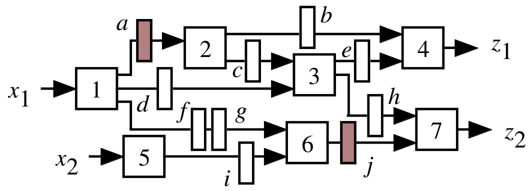

Figure 1. Acyclic sequential circuit S.

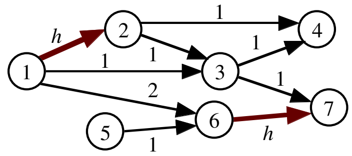

Figure 2. Topology graph of S: G.

Example 1: Consider a sequential circuit S illustrated in Fig. 1. In this figure, $1, 2, \ldots, 7$ are logic blocks, $b, c, \ldots, i$ are L-registers, and a and j, which are highlighted, are H-registers. The topology graph G of this circuit S is shown in Fig. 2. □

2.2 Time-Expansion Model (TEM)

Test generation for an acyclic sequential circuit can be performed by applying a combinational test generator to a *time-expansion model* of the circuit.

Definition 2 (Time-expansion graph (TEG)): Let S be an acyclic sequential circuit and let $G = (V, A, r)$ be the topology graph of S. Let $E = (V_E, A_E, t, l)$ be a directed graph, where V_E is a set of vertices, A_E is a set of arcs, t is a mapping from V_E to a set of integers, and l is a mapping from V_E to the set of vertices V in G. If graph E satisfies the following five conditions, graph E is said to be a *time-expansion graph (TEG)* of G.

C1(Logic preservation) The mapping l is a surjective, i.e.,

$$\forall v \in V, \exists u \in V_E \text{ s.t. } v = l(u).$$

C2(Input preservation) Let u be a vertex in E. For any direct predecessor v $(\in pre(l(u)))$ of u in G, there exists a vertex u' in E such that $l(u') = v$ and $u' \in pre(u)$. Here, $pre(v)$ denotes the set of direct predecessors of v.

C3(Time consistency) For any arc (u, v) $(\in A_E)$, there exists an arc $(l(u), l(v))$ such that $r(l(u), l(v)) = t(v) - t(u)$ or $r(l(u), l(v)) = h$.

C4(Time uniqueness) For any vertices u, v $(\in V_E)$, if $t(u) = t(v)$ and if $l(u) = l(v)$, then the vertices u and v are identical, i.e., $u = v$.

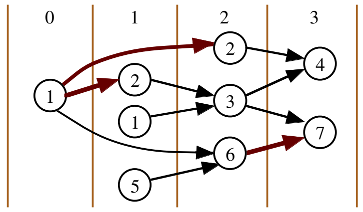

Figure 3. TEG of G: E_1.

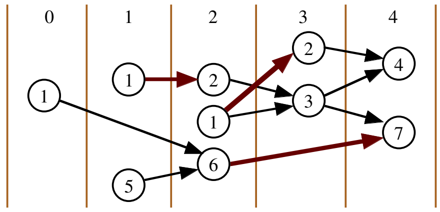

Figure 4. TEG of G: E_2.

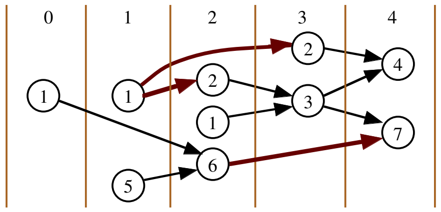

Figure 5. TEG of G: E_3.

C5(Hold consistency) For any pair of arcs (u_1,v_1), (u_2,v_2) $(\in A_E)$ such that $(l(u_1),l(v_1)) = (l(u_2),l(v_2))$ and $r(l(u_1),l(v_1)) = r(l(u_2),l(v_2)) = h$, if $t(u_1) > t(u_2)$, then $t(u_1) \geq t(v_2)$.

□

Example 2: Fig. 3, Fig. 4 and Fig. 5 show TEGs of topology graph G. In these figures, the number denoted in a vertex u is the label $l(u)$, and the number located at the top of each column denotes the value of the labels $t(u)$ of the vertices u in the column. □

Note that as shown in the above example, the TEG for a topology graph is not unique in general.

Definition 3 (Time-expansion model (TEM)): Let S be an acyclic sequential circuit, let $G = (V,A,r)$ be the topology graph of S, and let $E = (V_E,A_E,t,l)$ be a TEG of G. The combinational circuit $C_E(S)$ obtained by the following procedure is said to be the *time-expansion model (TEM)* of S based on E.

(1) For each vertex $u \in V_E$, let logic block $l(u)$ $(\in V)$ be the logic block corresponding to u.

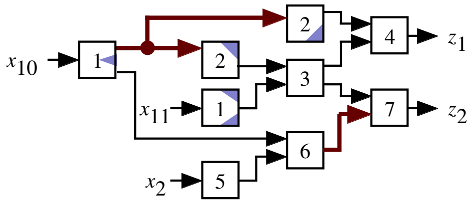

Figure 6. TEM of S based on E_1: $C_{E_1}(S)$.

(2) For each arc $(u,v) \in A_E$, connect the output of u to the input of v with a bus in the same way as $(l(u),l(v))$ $(\in A)$. Note that the connection corresponding to (u,v) has no register even if the connection corresponding to $(l(u),l(v))$ has a register (i.e., $r(l(u),l(v)) \neq 0$).

(3) Steps (1) and (2), if it is not reachable to any input of other logic blocks, then it is removed.

□

Example 3: Fig. 6 shows the TEM of sequential circuit S (Fig. 1) based on TEG E_1 (Fig. 3). In this figure, a highlighted part in a logic block represents a portion of the lines and gates removed by Step (3) in Def. 3. □

2.3 Test Generation with TEM

Here we consider the relationship between input/output sequences of an acyclic sequential circuit and input/output patterns of its TEM. Let S be an acyclic sequential circuit, and let $G = (V,A,r)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$ be a TEG of G, let $C_E(S)$ be the TEM of S based on E, and let $t_{\min}$ be the minimum of labels t in $C_E(S)$. An input pattern for $C_E(S)$ can be transformed into an input sequence for circuit S by the following procedure τ_S.

Definition 4 (Transformation procedure τ_S):

(1) Control input sequence I_H. Let $I_H(v',v,t)$ denote an input value which is applied to an H-register (v',v) $(\in A)$ at time t. For each arc $(u',u) \in A_E$ such that $r(l(u'),l(u)) = h$, let

$$I_H(l(u'),l(u),t-t_{\min}) = \begin{cases} L \text{ (LOAD mode)} & (t = t(u')) \\ H \text{ (HOLD mode)} & (t(u')+1 \leq t \leq t(u)-1) \end{cases}$$

Let the values $I_H(v',v,t)$ which are not defined by the above equation be X (don't care).

(2) Data input sequence I_S. For each logic block $u \in V_E$ in $C_E(S)$, let

$$I_S(l(u),t(u)-t_{\min}) = I_C(u),$$

Table 1. Input and output sequences for S obtained by transformation procedure τ_S.

Time		0	1	2	3
Data Input	x_1	I_{10}	I_{11}	X	X
	x_2	X	I_2	X	X
Control Input	Reg. a	L	H	X	X
	Reg. j	X	X	L	X
Output	z_1	X	X	X	O_1
	z_2	X	X	X	O_2

where $I_S(v,t)$ denotes an input-pattern applied to logic block v in S at time t, and $I_C(u)$ denotes an input-pattern applied to logic block u in $C_E(S)$.

□

Note that in the above procedure, a control input sequence is obtained only from a TEG E independent of an input-pattern for TEM $C_E(S)$.

Lemma 1: Let I_C be an arbitrary input-pattern for TEM $C_E(S)$, and let I_S and I_H be a data input sequence and a control input sequence obtained by τ_S, respectively. The output pattern $O_C(u)$ obtained from a logic block $u \in V_E$ by applying input pattern I_C to $C_E(S)$ is equal to the output pattern $O_S(l(u), t(u) - t_{\min})$ obtained from the corresponding logic block $l(u)$ at time $t(u) - t_{\min}$ by applying data input sequence I_S with control input sequence I_H.
(Proof.) See appendix. □

Example 4: Consider a TEM $C_{E_1}(S)$ (Fig. 6) of a sequential circuit S shown in Fig. 1. Suppose an input-pattern $I_C = (x_{10}, x_{11}, x_2) = (I_{10}, I_{11}, I_2)$ applied to $C_{E_1}(S)$ and the corresponding output-pattern is $O_C = (z_1, z_2) = (O_1, O_2)$. According to the labels t in TEG E_1 (Fig. 3), the patterns I_C and O_C are transformed into the sequences shown in Table 1 by procedure τ_S. Here, X denotes a don't-care value. □

Note that the length of the sequence obtained from a pattern for TEM $C_E(S)$ by procedure τ_S becomes $\max_{u \in V_E}\{t(u)\} - \min_{u \in V_E}\{t(u)\} + 1$.

Let I_S and I_H be a data input sequence and a control input sequence for acyclic sequential circuit S such that the sequences determine the output pattern $O_S(v,t)$ of a logic block v $(\in V)$ in S at time t, respectively. Here, a pattern that does not affect $O_S(v,t)$ in the input sequences I_S and I_H is considered as don't-care. Input sequences I_S and I_H for S can be transformed into a TEG E and an input-pattern I_C for the TEM $C_E(S)$ by the following procedure τ_C.

Definition 5 (Transformation procedure τ_C):

(1) TEG E. Create a TEG $E = (V_E, A_E, t, l)$ in which there exists a vertex $u \in V_E$ that satisfies the following conditions.
(1) $l(u) = v \wedge t(u) = t$, and
(2) For the control input value $I_H(v_1, v_2, t')$ applied to an H-register (v_1, v_2) $(r(v_1, v_2) = h)$ at time t',
if $I_H(v_1, v_2, t') = L$, then there exists a vertex $u_1 \in Pre(u)$ such that $l(u_1) = v_1 \wedge t(u_1) = t'$,
if $I_H(v_1, v_2, t') = H$, then there exists an arc (u_1, u_2) $(\in A_E)$ such that $u_1, u_2 \in Pre(u) \wedge t(u_1) < t' \wedge t(u_2) > t'$.
Here, $Pre(u)$ denotes the set of all predecessors of u.

(2) Input-pattern I_C. For every input pattern $I_S(v', t')$ applied to each logic block v' at time t', if $I_S(v', t')$ affects output $O_S(v,t)$, then for the logic block u' that satisfies $u' \in l^{-1}(v')$ and $t(u') = t'$, let $I_C(u') = I_S(v', t')$.

□

Lemma 2: Let v $(\in V)$ be an arbitrary logic block in acyclic sequential circuit S, and let I_S and I_H be a data input sequence and a control input sequence that are required to set the output of v to a pattern $O_S(v,t)$ at time t, respectively. Let E and I_C be a TEM and an input-pattern obtained from I_S and I_H by procedure τ_C, respectively. Let u $(\in V_E)$ be the logic block that corresponds to v by the first step (1) in procedure τ_C. The output pattern $O_C(u)$ obtained from the logic block u by applying the input pattern I_C to TEM $C_E(S)$ is equal to the output pattern $O_S(v,t)$.
(Proof.) See Appendix. □

Note that as shown in the above procedure τ_C, a TEG (or TEM) is obtained from a control input sequence applied to H-registers in a sequential circuit, independent of data input sequences.

Next, let us consider the relationship between faults in an acyclic sequential circuit and those in its TEMs. Here we consider single stuck-at faults only in logic blocks as those in an original sequential circuit. The stuck-at faults on lines between logic blocks and in registers can be considered to be equivalent to those on input/output lines of logic blocks.

Definition 6 (Fault in TEM): Let S be an acyclic sequential circuit. Let $G = (V, A, r)$ be the topology graph of S, let $E = (V_E, A_E, t, l)$ be a TEG of G, and let $C_E(S)$ be the TEM of S based on E. Let F be the set of faults in S, and let F_E be the set of faults in $C_E(S)$. Suppose a fault $f \in F$ in a logic block u in circuit S. Let $f_e \in F_E$ be the fault corresponding to fault f. Fault f_e is a multiple fault that consists of all the faults existing on the same line in every logic block $u \in l^{-1}(v)$. That is, if the number of logic blocks u such that $l(u) = v$ is just one, then the fault f_e is a single fault, otherwise, f_e is a multiple fault. □

Theorem 1: Let S be an acyclic sequential circuit, and let F be the set of faults in S. Let $G = (V, A, r)$ be the topology graph of S.

(1) A fault $f \in F$ is testable (or irredundant) in S if and only if there exists a TEG E of G such that the fault f_e ($\in F_E$) corresponding to f is testable in the TEM $C_E(S)$ based on E.

(2) A test pattern for a fault f_e ($\in F_E$) obtained using a TEM $C_E(S)$ can be transformed into a test sequence for the fault f ($\in F$) corresponding to fault f_e.

(Proof.) See Appendix. □

From this theorem, we can see that test generation for an acyclic sequential circuit can be performed by using several different TEMs. Furthermore, since TEMs are fully combinational, a combinational test generator can be used for the test generation provided that the test generator can deal with multiple faults. However, from Theorem 1, we can also have the following corollary.

Corollary 1: Let S be an acyclic sequential circuit. Let F be a set of faults in S. A fault $f \in F$ is untestable (or redundant) in S if and only if the fault corresponding to f_e is untestable in any TEM for S. □

Hence, in order to obtain a complete test sequence (i.e., to identify all testable faults) for a sequential circuit, we may have to perform test generation for *all* TEMs of the circuit. However, that is practically prohibitive. Therefore, in order to reduce the number of TEMs required for the test generation, we introduce *cover relation* of TEMs, and consider the TEMs used for complete test sets.

3 Sequential Circuits with Maximum TEM

3.1 Cover Relation of TEMs

Here we consider the relation between TEMs (or TEGs) obtained for an acyclic sequential circuit. Let S be an acyclic sequential circuit. Let $G = (V, A, r)$ be the topology graph of S, and let $E_1 = (V_1, A_1, t_1, l_1)$ and $E_2 = (V_2, A_2, t_2, l_2)$ be arbitrary TEGs of G. Let $C_{E_1}(S)$ and $C_{E_2}(S)$ be the TEMs based on E_1 and E_2 of S, respectively.

Definition 7 (Cover relation): TEG E_1 is said to *cover* TEG E_2 if, for any vertex $v_2 \in V_2$, there exists a vertex $v_1 \in V_1$ which satisfies the following two conditions.

(1) $l(v_1) = l(v_2)$.

(2) Let $V_1' = Pre(v_1)$ and let $V_2' = Pre(v_2)$, where $Pre(v)$ denotes the set of all predecessors of v. There exists a mapping $m : V_1' \to V_2'$ which satisfies the following two conditions.

(2.1) $l_1(v_1) = l_2(m(v_1))$.

(2.2) For any vertex $v_2' \in V_2'$,

$$\forall v_1' \in m^{-1}(v_2')\ [L_2(v_2') \supseteq L_1(v_1')],$$

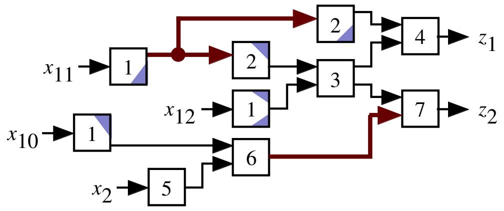

Figure 7. TEM of S based on E_3: $C_{E_3}(S)$.

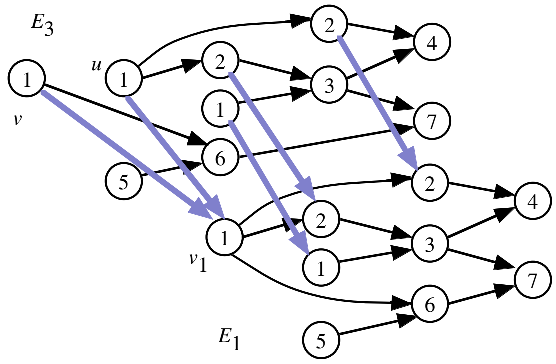

Figure 8. Mapping m from V_3 in E_3 to V_1 in E_1.

where $L_i(v') = \{v \in V | v = l_i(u), u \in suc(v') \cap V_i'\}$. Here, $suc(v)$ denotes the set of direct successors of v. That is, $L_i(v')$ denotes the set of logic blocks in V corresponding to those which are reachable from logic block v' in TEG V_i.

□

When a TEG E_1 covers a TEG E_2, we denote that $E_1 \succeq E_2$. Further, it is also said that TEM $C_{E_1}(S)$ covers TEM $C_{E_2}(S)$ ($C_{E_1}(S) \succeq C_{E_2}(S)$).

Example 5: Consider two TEMs $C_{E_1}(S)$ (Fig. 3) and $C_{E_3}(S)$ (Fig. 5) for the topology graph G (Fig. 2) of a sequential circuit S (Fig. 1). Suppose a mapping m as shown in Fig. 8. In this figure, a highlighted arrow from a vertex $v_3 \in V_3$ to a vertex $v_1 \in V_1$ denotes $m(v_3) = v_1$. For simplicity, unique correspondences such that the number of vertices $v_1 \in V_1$ whose labels $l(v_1)$ are the same vertex (in V of G) is just one are omitted. Since this mapping m which satisfies all the conditions in Def. 7, TEG E_3 covers TEG E_1. Note that $E_1 \not\succeq E_3$. □

The mapping m in the above definition represents the relationship between logic blocks corresponding to a logic block v ($\in G$) in a TEG E_1 and those corresponding to the same one v in a TEG E_2. When E_1 covers E_2, since the relation m is mapping from V_1 to V_2, multiple vertices in V_1 may correspond to one vertex in V_2. For example, there exist three and two vertices that are labeled with 1 in E_3 and E_1, respectively, and two of them in E_3 correspond to one vertex in E_1. Here, let u denote one of the two vertices, which is connected vertices labeled with two 2's, and let v denote the other vertex connected the vertex labeled with 6 in E_3. Further, let v_1 denote the vertex corresponding to u, v in E_1 by mapping m. By Condition C4 in Def. 2 (the definition of TEGs), in a TEG, for two different vertices u, v whose labels are the same, i.e., $l(u) = l(v)$, the labels $t(u)$ and $t(v)$ must be different (e.g., $t_3(u) = 1, t_3(v) = 0$). While vertex v_1 is reachable to a vertex labeled with 7 via two paths $(1,2,3,7)$ and $(1,6,7)$ in E_1, vertex u is reachable to the corresponding vertex labeled with 7 via a path $(1,2,3,7)$ and the other vertex v can reach the vertex 7 via a path $(1,6,7)$. This means that the number of logic blocks that affect a particular logic block in $C_{E_3}(S)$ (a covering TEM) is equal to or larger than that in $C_{E_1}(S)$ (a covered TEM). In other words, for any output-pattern $O(v'_1)$ obtained by applying an input-pattern I_1 to $C_{E_1}(S)$, the same output-pattern $O(v'_1)$ can be obtained from the corresponding logic block v'_3 in $C_{E_3}(S)$ by applying the input-pattern I_3 that is obtained from I_1 according to mapping m as follows.

Example 6: Suppose an output-pattern $(z_1, z_2) = (O_1, O_2)$ for an input-pattern $(x_{10}, x_{11}, x_2) = (I_a, I_b, I_c)$ in $C_{E_1}(S)$ (Fig. 6). The same output-pattern $(z_1, z_2) = (O_1, O_2)$ can be obtained by applying $(x_{10}, x_{11}, x_{12}, x_2) = (I_a, I_a, I_b, I_c)$ to $C_{E_3}(S)$ (Fig. 7). □

As shown in the above example, if a TEM C_1 covers another TEM C_2, C_1 can 'simulate' C_2. On the other hand, by definition Def. 6, for any fault in an acyclic sequential circuit, the corresponding fault is defined in either TEM of C_1 and C_2. Thus, we can form the following conjecture.

Conjecture 1: Let S be an acyclic sequential circuit. Let C_1 and C_2 be TEMs of S. Let F_1 and F_2 be the set of faults in C_1 and C_2, respectively (Def. 6). If TEM C_1 covers TEM C_2, the following holds: If a fault f_2 $(\in F_2)$ in C_2 is testable, fault f_1 $(\in F_1)$ in C_1 corresponding to f_2 is also testable. □

We believe that this conjecture holds as a theorem, though the proof has not obtained yet.

For any pair of TEGs E_1 and E_2 for an acyclic sequential circuit S, if $E_1 \succeq E_2$ and $E_2 \not\succeq E_1$, E_1 is said to cover E_2 *properly*, and it is denoted by $E_1 \succ E_2$. For a TEG E, if there exists no TEG E' such that $E' \succ E$, TEG E is called *maximal*. Then, we can obtain the following corollary.

Corollary 2: A fault f is testable in an sequential circuit S if and only if there exists a maximal TEM in which f_m corresponding to f is testable. □

This implies that test generation for all the maximal TEMs of an acyclic sequential circuit is necessary and sufficient to obtain a complete test sequence for all testable faults in the circuit.

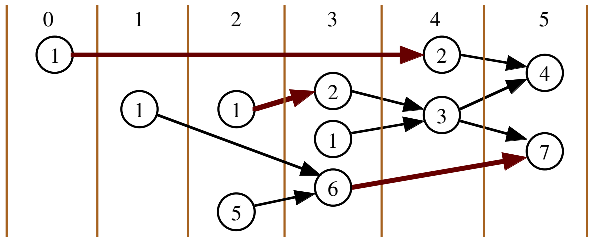

Figure 9. Example of inconsistent graph.

3.2 Class of Max-Testable Structure

In the above discussion, we showed that test generation for all the maximal TEMs of an acyclic sequential circuit is necessary and sufficient to obtain a complete test sequence for the circuit. In general, however, there exist several maximal TEMs for an acyclic sequential circuit.

Example 7: Consider TEMs for a sequential circuit S shown in Fig. 1. As shown in Figs. 3, 4 and 5, several TEMs for S can be constructed. As mentioned previously, $E_3 \succ E_1$, but $E_2 \not\succeq E_3$ and $E_3 \not\succeq E_2$. Further, there is no TEM which covers either E_2 or E_3 properly. As a result, all the maximal TEMs for S are E_2 and E_3. □

If the number of maximal TEMs is one, i.e., there exists the *maximum* TEM for a sequential circuit, a complete test set for the circuit can be generated only by performing combinational test generation for the maximum TEM. If a sequential circuit has the maximum TEM, the sequential circuit is called *max-testable*.

Example 8: Consider sequential circuit S (Fig. 1) again. Suppose a directed graph as shown in Fig. 9. We can make a mapping m described in Def. 7 from the vertex set in this graph to that in either of maximal TEGs E_2 and E_3. This graph, however, is not a TEG for S because it does not satisfy Condition C5 in Def. 2, i.e., there exists no control input sequence corresponding to the graph: an H-register a cannot load a value at time 2 while holding a value loaded at time 0 to be used at time 4. □

As shown in the above example, the condition C5 in Def. 2 is for more than one arcs that correspond to a certain H-register in an acyclic sequential circuit. Such arc duplication for an H-register is possible in a TEG when there exist more than one paths from the H-register to an primary output in the circuit. Hence, here we consider a class of max-testable sequential circuits as follows.

Definition 8 (Path-adjustable structure): Let S be an acyclic sequential circuit. Let $G = (V, A, r)$ be the topology graph of S. Let $P(u, v)$ denote a set of paths from u to v $(u, v \in V)$. If G satisfies the following condition, sequential circuit S is said to be *path-adjustable*.
(CPA) Let V' $(\subseteq V)$ be a set of vertices which are reachable from some arc $a_h (\in A)$ such that $r(a_h) = h$ (H-register). Let

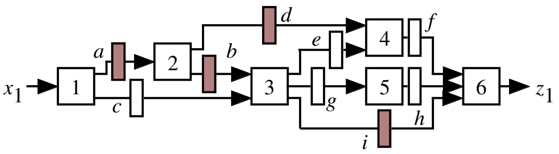

Figure 10. Sequential circuit S_2.

u, v be any pair of vertices in V'. For any pair of paths $p, q \in P(u, v)$,

(1) if $H(p) = H(q)$, then $d(p) = d(q)$, else

(2) if $H(p) \neq H(q)$, then
$H(p) \cap H(q) \neq \phi \Rightarrow H(p) \subset H(q) \vee H(p) \supset H(q)$.

Here $d(p)$ denotes the number of arcs a $(\in A)$ such that $r(a) \in Z^+$ (L-register) in a path p, and $H(p)$ denotes the set of arcs a such that $r(a) = h$ (H-register) in a path p. □

In the above condition CPA, the former case (1) means that arc duplication for arc a_h does not occur in any TEG of G. On the other hand, the latter case (2) means a sufficient condition for existence of H-registers for which control signals are *'adjustable'* to make a maximum TEG while Condition C5 in Def. 2 for arc a_h is satisfied. That is, even if the control input sequence for all the H-registers on a path p is determined prior to that on the other q, some H-register to satisfy Condition C5 still remains for q. Note that in neither case, i.e., in the case when $H(p) \cap H(q) = \phi$, the control input sequence for any H-register on a path does not affect that for the others to satisfy Condition C5.

Example 9: Consider a sequential circuit S_2 shown in Fig. 10. In this figure, a, b, d and i are H-registers, and the others are L-registers. For example, let us focus on an H-register a. There exist four paths to be considered for a: $p_1 = (2, d, 4, f, 6)$, $p_2 = (2, b, 3, e, 4, f, 6)$, $p_3 = (2, b, 3, g, 5, h, 6)$ and $p_4 = (2, b, 3, i, 6)$. Then, $H(p_1) = \{d\}, H(p_2) = \{b\}, H(p_3) = \{b\}$ and $H(p_4) = \{b, i\}$. For p_1 and p_2, $H(p_1) \cap H(p_2) = \phi$, this is in neither case. For p_2 and p_3, $H(p_2) = H(p_3) = \{b\}$ and $d(p_2) = d(p_3)$, i.e., case (1). For p_2 and p_4, $H(p_2) \subset H(p_4)$, i.e., case (2). Similarly, all the other pairs of paths in this circuit S_2 also satisfy the condition CPA, and hence S_2 is path-adjustable. Note that a sequential circuit S (Fig. 1) is not path-adjustable. As a result, we can obtain the maximum TEM for S_2 as shown in Fig. 11. The control input sequence obtained from the TEM (by procedure τ_S) is $I_H(a) = (L, L, L, H, X, X, X)$, $I_H(b) = (X, X, L, H, L, X, X)$, $I_H(d) = (X, L, H, H, H, X, X)$, $I_H(h) = (X, X, X, X, X, L, X)$. □

From the above discussion, we have the following conjecture.

Conjecture 2: A path-adjustable sequential circuit is max-testable. □

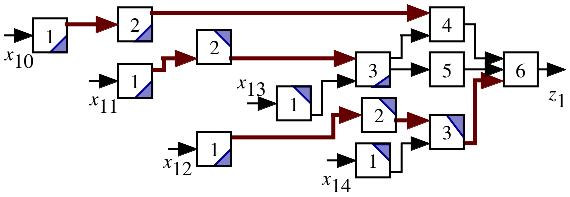

Figure 11. Maximum TEM for S_2.

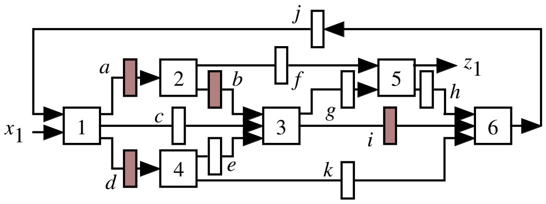

Figure 12. Sequential circuit S_3.

We believe that this conjecture also holds as a theorem, though the proof has not obtained yet.

3.3 DFT Based on Path-Adjustable Structure

From Conjecture 2, we can see that for any sequential circuit, by selecting a sufficient set of scan registers so that the resulting kernel is path-adjustable, a complete test sequence for the circuit can be obtained by using a combinational test generator for only the maximum TEM of the kernel (provided that the test generator can deal with multiple faults). On the other hand, from Def. 8, we have the following corollary.

Corollary 3: All the following sequential circuits are path-adjustable.

(1) balanced structures [5].

(2) internally-balanced structures [7].

(3) acyclic sequential circuits without H-registers.

□

Therefore, for a sequential circuit, the hardware overhead of the partial scan based on path-adjustable structure is smaller than that based on the structures mentioned in Corollary 3.

Example 10: Consider a sequential circuit S_3 shown in Fig. 12. In this figure, a, b, d and i are H-registers, and the others are L-registers. In the partial scan design based on path-adjustable structure, the minimum number of scan registers is two, e.g., by scanning L-registers j and k, the resulting kernel becomes path-adjustable. Note that there is an alternative DFT solution: if one L-register j is scanned and another L-register k is replaced with an H-register, then the resultant circuit is also path-adjustable.

On the other hand, in the partial scan design based on balanced structure, the minimum number of scan registers is five, e.g., the set of registers to be scanned is $\{b,c,e,f,k\}$. When the kernel is made an acyclic structure without H-registers, the minimum number of scan registers is also five, e.g., $\{a,b,d,h,i\}$. □

Therefore, it is seen that we can obtain complete test sequences for sequential circuits with low hardware overhead based on max-testable structure.

4 Conclusions and Future Works

In this paper, we presented a method of test generation for acyclic sequential circuits with *hold* registers. A *complete* test set for an acyclic sequential circuit can be obtained by applying a *combinational* test generator to all the *maximal time-expansion models (TEMs)* of the circuit. As a class of *max-testable* sequential circuits, referring to acyclic sequential circuits for which the number of maximal TEMs is one, i.e, the *maximum* TEM exists, we introduced *path-adjustable* structure. The class of path-adjustable sequential circuits properly includes several known classes of acyclic sequential circuits such as balanced structures and acyclic sequential circuits without hold registers for which test generation can be also performed by using a combinational test generator. Therefore, the hardware overhead for partial scan based on our path-adjustable structure is substantially smaller than that based on balanced or acyclic sequential structure without hold registers.

As future works, several issues are remaining.

- The condition in the definition of path-adjustable structure is a sufficient one for existence of the maximum TEM for acyclic sequential circuit. We believe that there exists a lager class of max-testable sequential circuits, and hence the hardware overhead of DFT for complete test sequences can be reduced further.
- We are now investigating an algorithm for finding an optimal partial scan / hold register insertion based on max-testable structure with minimum hardware overhead.
- The length of test sequences obtained from test generation using TEMs depends on the structure of the TEMs. Hence, optimal TEMs which minimize the length of resulting test sequences should be found.

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Appendix

Proof of Lemma 1. Let u' ($\in pre(u)$) be a logic block connected to an input of logic block u. By Condition C1, in S, there exist logic blocks $l(u), l(u')$ corresponding to u, u' respectively, and by Condition C2, the logic block u' is connected to the input of logic block u. By procedure τ_S, an input pattern $I_C(u')$ for u' is transformed into the input pattern $I_H(l(u'), t(u') - t_{\min})$ for $l(u')$ at time $t(u') - t_{\min}$. From Condition C4, we can say that the number of patterns to be applied to $l(u')$ at time $t(u') - t_{\min}$ is just one. If the two logic blocks $l(u)$ and $l(u')$ are connected directly or through one or more L-registers, the effect of applying $I_S(l(u'), t(u') - t_{\min})$ reaches $l(u)$ after $r(l(u'), l(u))$ clock cycles. Since $r(l(u'), l(u))$ denotes the number of L-registers between $l(u')$ and $l(u)$, by Condition C3, we can say that $(t(u') - t_{\min}) + r(l(u'), l(u)) = t(u) - t_{\min}$. Or else, i.e., if the two logic blocks are connected though an H-register, the output-pattern obtained from logic block $l(u')$ by applying $I_S(l(u'), t(u') - t_{\min})$ at

$t(u') - t_{\min}$ is loaded into the H-register $(l(u'), l(u))$. By Condition C5, the contents of the register is not update by other LOAD signals, and kept until $t(u) - t_{\min}$ by the control input sequence I_H. $\square$

Proof of Lemma 2. Let $u \in V_E$ be the logic block that is created in $C_E(S)$ by step (1) in procedure τ_C. Let v' ($\in pre(v)$) be a logic block connected to an input of logic block v. By Condition C2, the logic block u' ($\in l^{-1}(v')$) corresponding to v' is connected to an input of u. By step (2) in procedure τ_C, an input-pattern $I_S(v', t')$ applied to v' at time t' is transformed into the input-pattern $I_C(u_p)$ for u_p. If two logic blocks v and v' are connected directly or through one or more L-registers, the time t' when input-pattern $I_S(v', t')$ is applied to obtain output-pattern $O_S(v, t)$ from logic block v at t must be $t - r(v', v)$. Note that $r(v', v)$ denotes the number of L-registers between v' and v. By Condition C3, $t(u') = t(v) - r(v', v) = t - r(v', v)$. If two logic blocks v and v' are connected through an H-register, the output-pattern of logic block v' is loaded into the H-register (v', v) at t' by a control input value $I_H(v', v, t') = L$. By step (1) in procedure τ_C, according to the control input value $I_H(v', v, t') = L$, the corresponding vertex u' which is labeled $t(u') = t'$. From Conditions C4 and C5 and step (1) in procedure τ_C, we can say that the number of logic blocks u' such that $t(u') = t' \vee l(u') = v'$ is just one in $C_E(S)$. $\square$

Proof of Theorem 1. Let E be a TEG of G, and Let $C_E(S)$ be the TEM based on E. Let f be a fault in S, and let f_e be the fault corresponding to f in $C_E(S)$. Let S^f be a faulty circuit with f of S. Let $C_E^{f_e}(S)$ be a faulty circuit with f_e of $C_E(S)$. By Def. 6, fault f_e is a multiple fault that consists of faults in every logic block $l^{-1}(v)$ corresponding to a logic block v ($\in V$) in which exists fault f. Hence, the structure of $C_E^{f_e}(S)$ is the same as that of $C_E(S^f)$ for S^f based on TEG E.

Therefore, by Lemma 2, for a test sequence T_S for a fault f in S, there exists a TEM E that corresponding to the control input sequence in T_S, and there exists a test pattern obtained from T_S by procedure τ_C can detect the fault f_e corresponding to f. Further, by Lemma 1, a test pattern t_C for a fault f_e in the TEM $C_E(S)$ based on a TEG E can be transformed into a test sequence that can detect f corresponding to f_e in S by procedure τ_S. $\square$