Partial Scan Design Methods Based on Internally Balanced Structure

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Abstract— In this paper, we theoretically and experimentally show the effectiveness of partial scan design based on internally balanced structure, which is a sequential circuit capable of generating tests with a combinational test generation algorithm. Moreover, we introduce a method of extended partial scan design, which transforms a sequential circuit into an easily testable sequential circuit by replacing part of not only flip-flops by scan flip-flops but also wires by bypass flip-flops in the sequential circuit, and propose a method of extended partial scan design based on internally balanced structure. We present an algorithm for finding a set of flip-flops and wires in order to minimize the area overhead for the extended partial scan design. We consider the test procedure for the kernel circuit using the scan path and the additional circuit by scan design with the partial scan design and the extended partial scan design based on internally balanced structure and demonstrate the effectiveness of the test procedures. Experimental results for benchmark circuits show that the proposed partial scan design and extended partial scan design can be implemented with low area overhead.

Keywords: Sequential circuits, test generation, internally balanced structure, bypass flip-flops, extended partial scan design

I. Introduction

Test generation for a sequential circuit is generally difficult and intractable problem when the scale of the circuit is larger. To solve this problem, full scan design technique, which replaces all the flip-flops by scannable flip-flops (scan flip-flops) in a sequential circuit, have been proposed [1][2]. In full scan design, the circuit which excludes scan flip-flops (*kernel circuit*) is a combinational circuit so that it is capable of generating tests with a combinational test generation algorithm (*capable of combinational test generation*) and achieves almost complete fault efficiency. However, the full scan design technique leads to an overhead in circuit area. Partial scan design, which replaces part of flip-flops by scan flip-flops in a sequential circuit, is one of techniques which implement an easily testable circuit with low area overhead. Partial scan design techniques which require sequential test generation [3][4] for the sequential kernel circuit, however, are still difficult to achieve high fault efficiency. On the other hand, partial scan design such that the kernel circuit is a *balanced structure*, which is a sequential circuit capable of combinational test generation, has been proposed [6]. We have proposed a sequential circuit with *internally balanced structure*, which is a circuit extending balanced structure as a sequential circuit capable of combinational test generation, and its application to partial scan design [7].

In this paper, to reduce further area overhead, we introduce a method of *extended partial scan design*, which replaces part of not only flip-flops by scan flip-flops but also wires by *bypass flip-flops*[2][8][10] in a sequential circuit, and propose a method of extended partial scan design such that the kernel circuit is an internally balanced structure. We present an algorithm for finding a set of flip-flops and wires in order to minimize the area overhead for the extended partial scan design. We consider the test procedure for the kernel circuit using the scan path and the additional circuit by scan design with the partial scan design and the extended partial scan design based on internally balanced structure and demonstrate the effectiveness of the test procedures. Experimental results for ISCAS'89 benchmark circuits show that the proposed partial scan design and extended partial scan design can be implemented with low area overhead.

II. Sequential Circuits Capable of Combinational Test Generation

When a sequential circuit has some feedback loops, it is not capable of combinational test generation [3]. In this section, we restrict the target circuit to a sequential circuit with acyclic structure (with no feebback loops). We restrict flip-flops (FF's for short) to DFF's without loss of generality. In the next section, we consider general sequential circuits with feedback loops.

On a fanout point in a circuit, the wire corresponding to an input of the fanout point is called the *fanout stem*, and the wires corresponding to outputs of the fanout point are

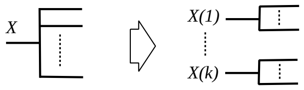

Fig. 1. Separation of primary inputs

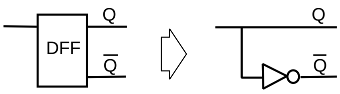

Fig. 2. Deletion of Flip-Flops

called the *fanout branches.* The *sequential depth* of a path is the number of flip-flops along the path. The *sequential depth of a sequential circuit* is the maximum sequential depth among the paths from primary inputs to primary outputs in the sequential circuit. Let x be a primary input and let x_i and x_j be its two fanout branches. If there are no paths with the same sequential depth form x_i and x_j to a primary output z_k then x_i and x_j are said to be *separable.*

Combinational transformation (C-transformation)[7] : The transformation consisting of the two following operations for an acyclic sequential circuit S are called the *Combinational transformation* (*C-transformation*), and the combinational circuit after the transformation is expressed as $C(S)$.

(1) For a primary input having some fanout branches, let X be a set of fanout branches of the primary input. Find the minimal partition π for X which satisfies : If fanout branch x_i and x_j belong to different blocks $X(i)$ and $X(j)$, respectively by partition π (i.e., $x_i \in X(i)$, $x_j \in X(j)$; $X(i) \neq X(j)$), x_i and x_j are separable. Create new inputs for every partitioned blocks and separate the original primary inputs. (See Figure 1.)

(Note: When separating a primary input, a fault in its fanout stem is considered as multiple faults exsiting in all the fanout branches simultaneously.)

(2) Replace each FF in S by a wire. (When the negative output of a FF is used, add an inverter. See Figure 2.) □

Capability of combinational test generation[7] :

Let S be an acyclic sequential circuit and let $C(S)$ be the C-transformed combinational circuit. The sequential circuit S is said to be *capable of combinational test generation* when it satisfies : a fault f in S is testable in S if and only if the corresponding fault f_c in $C(S)$ is testable in $C(S)$.

Sequential circuits capable of combinational test generation are the following :

Balanced structure[6] : If all paths for any input-output pairs in a sequential circuit S have the same sequential depth then S is said to be a *balanced structure.* (See Figure 3.)

Internally balanced structure[7] : If the circuit S' transformed from S by using only the rule (1) of C-transformation is a balanced structure, then S is said to be an *internally balanced structure.* (See Figure 4.)

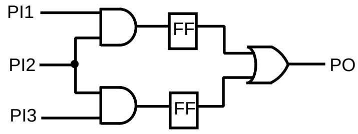

Fig. 3. Example of balanced structure

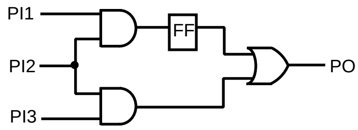

Fig. 4. Example of internally balanced structure

Since balanced sequential circuits have no separable primary inputs, only the rule (2) of C-transformation is carried out. From the above definition, it is clear that internally balanced structures belong to a larger class of sequential circuits than balanced structures.

III. Internally Balanced Partial Scan Design

Next we consider a general sequential circuit with feedback loops. Partial scan design such that the rest circuit excluding scan FF's (the kernel circuit) is an internally balanced structure is called *internally balanced partial scan design.* Internally balanced partial scan design enables test generation using only a combinational test generation algorithm. This issue is discussed further in Section VII. In Section VIII, experimental results for benchmark circuits show that internally balanced partial scan design can be implemented with low area overhead.

IV. Extended Partial Scan Design

We define *removing* of an elment e (FF or wire) in S for a sequential circuit S as replacing the input to e by a primary output of S and the output from e by a primary input of S and separating the element e from S. The replaced primary input and primary output are called *pseudo input* and *pseudo output*, respectively. The operation is expressed as operator $-$. For a set of elements E in S, $S - E$ defines the circuit removing all elements in E from S.

Let F and L be a set of flip-flops and a set of wires in a sequential circuit S, respectively. Given a set of the elements $E = \{FF_1, \ldots, FF_n, l_1, \ldots, l_m\}$ (provided $FF_i \in F$ $(i = 1, \ldots, n)$, $l_j \in L$ $(j = 1, \ldots, m)$) in S, $S - E$ is called the *kernel circuit with respect to* E, and FF's and wires in E are called *external FF's* and *external wires*, respectively. (See Figure 5.)

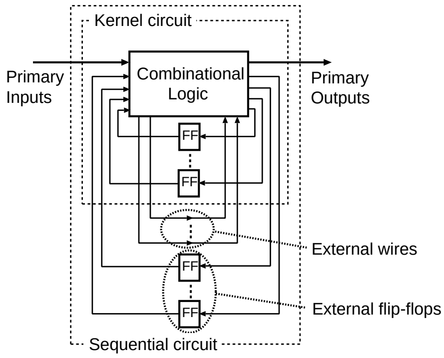

Fig. 5. Kernel circuit

TABLE I
Mode of operation and control line

	S-FF	B-FF	
	S	B_1	B_2
Normal mode	0	X	0
Load mode	0	0	1
Shift mode	1	1	1

Most partial scan design techniques replace only FF's by scan FF's and generate test patterns for the kernel circuit which excludes scan FF's. However, some partial scan design methods have also been proposed, which replace not only FF's by scan FF's but also wires by *bypass FF's* (which work like scan FF's). As shown in Figure 6, the partial scan design which replaces external FF's by scan FF's and external wires by bypass FF's is said to be *extended partial scan design.*

For the circuit with extended partial scan design, scan FF's and bypass FF's are called *extended scan FF's* generically.

The structures of each scan FF and bypass FF (S-FF and B-FF for short, respectively) are considered as in Figure 7 and Figure 8, respectively. Each S-FF and B-FF have three operation modes; the *normal mode*, the *load mode*, and the *shift mode*, according to the values of the control lines of the multiplexers in each FF as shown in Table I.

In the *normal mode*, each S-FF works as a DFF and each B-FF works as a wire as in Figure 6 (a). In the *load mode*, data are read from the data input of each FF during every clock cycle. In the *shift mode*, test patterns are scanned in each FF and the value of each FF is scanned out simultaneously through the scan path

Hold of FF's means the operation in which they retain their value across consecutive clock cycles. This operation mode is called the *hold mode.* Each extended scan FF in extended partial scan design is assumed to have the hold mode.

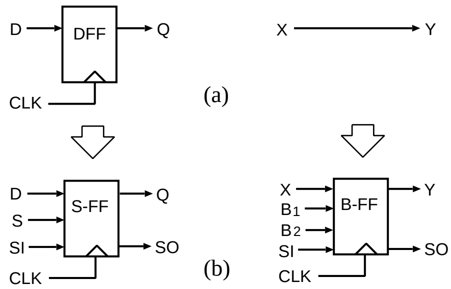

Fig. 6. Extended partial scan design

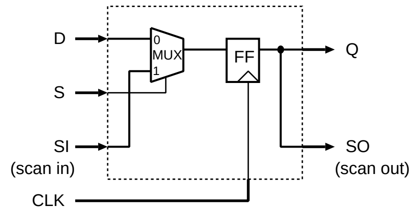

Fig. 7. Structure of scan flip-flop

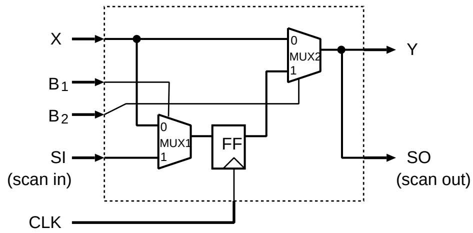

Fig. 8. Structure of bypass flip-flop

Let k_1 be the area overhead due to replacing a FF by a S-FF and let k_2 be the area overhead due to replacing a wire by a B-FF. Then, the total *area overhead* with extended partial scan design is expressed by the following exression :

The total area overhead
$= k_1 \times$ (the number of external FF's)
$+ k_2 \times$ (the number of external wires)

The ratio of k_1 to k_2 is, for example, 3 : 12 provided the hardware amount of a multiplexer and a FF are 3 and 6 gates, respectivelty, as the reference[9].

Compared to partial scan design scanning only FF's, extended partial scan design has more freedom to select scan elements and hence low area overhead is expected for its implemetation.

V. Internally Balanced Extended Partial Scan Design

For general sequential circuits, extended partial scan design such that the kernel circuit is an internally bal-

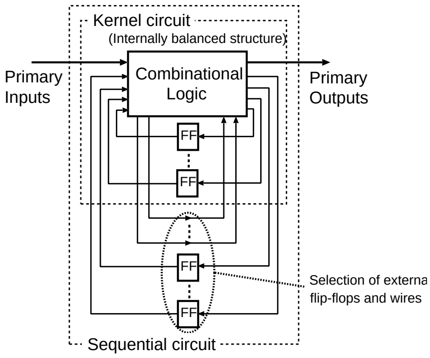

Fig. 9. Extended scan FF selection problem

anced structure enables test generation using only a combinational test generation algorithm like internally balanced partial scan design. This issue is discussed further in Section VII.

Extended partial scan design such that the kernel circuit is an internally balanced structure is called *internally balanced extended partial scan design.* In Section VI, We present an algorithm for finding a set of external FF's and external wires in order to minimize the area overhead for internally balanced extended partial scan design.

VI. Extended Scan FF's Selection Problem

The problem to find a set of external FF's and external wires in order to minimize the area overhead when the kernel circuit is an internally balanced structure for a given sequential circuit is called *extended scan FF's selection problem.* (See Figure 9.)

We consider a method to solve the extended scan FF's selection problem by dividing into the two following steps. However optimal solutions for the individual steps do not imply an optimal overall solution. Dividing the problem has the advantage of being able to transform the problem into the easy one and to use existing algorithms by simple modification.

1. *Acyclic structure*

Select a set of external FF's and external wires to minimize the area overhead such that the kernel circuit is an acyclic structure.

2. *Internally balanced structure*

For the acyclic kernel circuit obtained by Step 1,

(2-1) Separate primary inputs whose fanout branches are separable. (except pseudo inputs in the kernel circuit)

(2-2) Select a set of external FF's and external wires to minimize the area overhead such that the kernel circuit is a balanced structure.

We construct the following graph model for analyzing a sequential circuit to solve the problem.

Definition 1 : *A circuit topology graph* (CTG) for a sequential circuit S is a directed graph $G = (V, A, w)$.

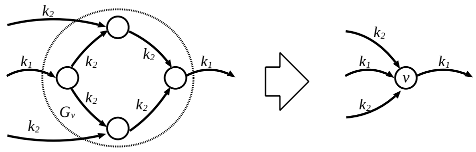

Fig. 10. Transformation rule of CTG

V is the set of nodes representing gates, fanout points, primary inputs and primary outputs in S.

$A \subset V \times V$ is the set of arcs representing FF's and wires in S (Each arc represent a connection in S).

$w : A \rightarrow Z^+$ (positive integers) defines the weights of the arcs. (FF's are of weight k_1 , and wires are of weight k_2, where k_1 is the area overhead due to replacing a FF by a S-FF and k_2 is the area overhead due to replacing a wire by a B-FF.) □

A CTG G can be transformed into a graph $\widehat{G}$ which has less nodes by applying the following transformation rule. As is evident from the transformation rule, the original graph G and the transformed graph $\widehat{G}$ have their solutions with the same area overhead for the extended scan FF's problem.

Transformation rule : Let G_v be an acyclic subgraph of a CTG G which consist of only nodes corresponding to gates and fanout points (except primary inputs and outputs) and weight k_2 arcs corresponding to wires. Let w_i be the sum of the weights of the incoming arcs in G_v and let w_o be the sum of the weights of the outgoing arcs in G_v. Let m_v be the minimum sum of the weights of the arcs needed to cut all directed paths in G_v. If there are paths from each input to all outputs in G_v, and

$$m_v \geq min\{w_i, w_o\}$$

then G_v will be merged into a node v as in Figure 10. □

Using the above graph model, the procedure to select external FF's and external wires such that the kernel circuit is an internally balanced structure can be described as follows.

Step 1. Transform the CTG G for a sequential circuit S into an CTG $\widehat{G} = (V, A, w)$ by applying the tranformation rule.

Step 2. Transform $\widehat{G}$ into an acyclic CTG G_A by removing a set of arcs R_A such that $\sum_{a \in R_A} w(a)$ is minimized.

Step 3. Transform G_A into a CTG $\widetilde{G}_A$ by separating primary inputs whose fanout branches are separable.

Step 4. Transform $\widetilde{G}_A$ into a balanced CTG G_B by removing a set of arcs R_B such that $\sum_{a \in R_B} w(a)$ is minimized.

As a result, $R = R_A \cup R_B$ is the desired set of arcs corresponding to external FF's and external wires.

At the above Step 2, a set of arcs R_A such that $\sum_{a \in R_A} w(a)$ is minimized is obtained by applying weighted MFAS (Minimum Feedback Arc Set) algorithms. In this case, assign k_1 (FF) or k_2 (wire) to each arc weight.

The operation to separate primary inputs at the Step 3 corresponds to the C-transformation (1) and is carried out as follows. That is, for all fanout branch pairs (x_i, x_j) of each primary input x, check whether there is a path with the same sequential depth from x_i and x_j to a primary output z_k. If such a path exists (x_i and x_j are not separable), x_i and x_j are put in the same set. Otherwise, they are put in different sets. As a result, new primary inputs for every created set are provided.

At the Step 4, a set of arcs R_B such that $\sum_{a \in R_B} w(a)$ is minimized is obtained by the procedure modifying the balancing procedure in the reference [6]. The balancing procedure in [6] assigns the bit width of the corresponding register to each arc weight. This procedure is applicable to the above balancing problem by replacing each arc weight by k_1 (FF) or k_2 (wire).

VII. Test Procedure for Circuit with Partial Scan Design

The test procedure for the circuit with internally balanced partial scan design and internally balanced extended partial scan design consists of testing the kernel circuit using the scan path and testing the additional circuit by scan design. In this section, we consider the test procedure and show its effectiveness for the circuit with internally balanced partial scan design and internally balanced extended partial scan design. Although the below issue is discussed about the circuit with internally balanced extended partial scan design, it is applicable to the circuit with internally balanced partial scan design if one consider the case there are no B-FF's.

Let S be a sequential circuit. Let S_{DFT} be the circuit with internally balanced extended partial scan design for S. Let S_K be the circuit removing extended scan FF's for S_{DFT} (the kernel circuit with internally balanced structure). Let $C(S_K)$ be the C-transformed circuit for S_K.

In order to test the circuit with extended partial scan design like S_{DFT} for a sequential circuit S, it is required to test all detectable faults in S_{DFT}. Faults in S_{DFT} corresponding to S_K are called *internal faults* in S_{DFT}. Faults in S_{DFT} but not in S_K (faults of extended scan FF's in S_{DFT}) are called *external faults* in S_{DFT}. Testing for each type of faults is described as follows.

A. Testing for Internal Faults

Let f_{DFT} be an internal fault in S_{DFT}, let f_K be the corresponding fault in S_K and let f_C be the corresponding fault in $C(S_K)$. f_{DFT} , f_K, and f_C are one-to-one correspondence each other.

For the circuit S_{DFT} with extended partial scan design such that the kernel circuit S_K is an internally balanced structure, the test sequence for an internal fault f_{DFT} in S_{DFT} is obtained as follows :

1. Generate the test pattern for the fault f_C in $C(S_K)$ corresponding to f_{DFT} by using a combinational test generation alrorithm.
2. Transform the generated test pattern into the test sequence in S_K.
3. Transform the test sequence in S_K into the test sequence in S_{DFT}.

The above procedure from 1 to 3 is discussed in detail later. On this procedure, the test generation problem for f_{DFT} in S_{DFT} results in the one for f_C in $C(S_K)$. In order to guarantee test generation using this, it is required to show that : a fault f_{DFT} in S_{DFT} is testable in S_{DFT} if and only if the corresponding fault f_C in $C(S_K)$ is testable in $C(S_K)$. This is shown by the following theorem.

From the reference [7], if a sequential circuit S_K is an internally balanced structure then S_K is capable of combinational test generation, therefore, this leads to the next theorem.

Theorem 1 : Let S_K be a sequential circuit with internally balanced structure. a fault f_K in S_K is testable in S_K if and only if the corresponding fault f_C in $C(S_K)$ is testable in $C(S_K)$. □

By Theorem 1, when S_K is an internally balanced structure, the procedure that the test pattern combinationally generated in $C(S_K)$ is transformed into the test sequence in S_K and in S_{DFT} is described as follows.

Procedure 1 : Test generation in $C(S_K)$ First, obtain $C(S_K)$ by applying the C-transformation to S_K. Since $C(S_K)$ is a combinational circuit, if the fault f_C corresponding to f_K is testable in $C(S_K)$, then the test pattren for f_C is obtained using a combinational test generation algorithm. (if f_K is redundant in S_K, then f_C is redundant in $C(S_K)$ (Theorem 1), the test pattern for f_C does not exist) When the test pattern for f_C is obtained, let T_C be this test pattern.

Procedure 2 : Test sequence in S_K Let d be the sequential depth of S_K. Then the length of the test sequence T_K in S_K is d. Let f_C be detected at an output (primary output or pseudo output) z_k in $C(S_K)$ by the test pattern T_C. In order that the fault f_K corresponding to f_C can be detected at an output z_k in S_K during clock cycle $d+1$, determine the values of primary input x_i $(i = 1, 2, \ldots, m)$ and pseudo input y_p $(p = 1, 2, \ldots, l)$ in the test sequence T_K as follows :

(1) Determining the values of primary input x_i $(i = 1, 2, \ldots, m)$

(1-a) Case where x_i is a separable primary input :

The sequential depth from each x_i to z_k is uniquely determined. Assign the value of primary input x_i in test pattern T_C to the vlaue of primary input x_i in test sequence T_K during clock cycle $d + 1 - d_{ik}$.

(1-b) Case where x_i is not a separable primary input :

Let primary input x_i in S_K be divided into primary inputs x_{i1}, x_{i2}, …, x_{in} in $C(S_K)$. Since S_K is an internally balanced structure, the sequential depth from each x_{ij} $(j = 1, 2, \ldots, n)$ to z_k is uniquely determined and let d_{ijk}

TABLE II
TEST PATTERN T_C AND TEST SEQUENCE T_K

(a) T_C

Input	*Value*
x_1	a_1
$\vdots$	$\vdots$
x_i	a_i
$\vdots$	$\vdots$
x_{h1}	a_{h1}
x_{h2}	a_{h2}
$\vdots$	$\vdots$
x_m	a_m
y_1	b_1
$\vdots$	$\vdots$
y_p	b_p
$\vdots$	$\vdots$
y_l	b_l

(b) T_K

	Clock cycle t										
Input	1	$\cdots$	$d+1-d_{ik}$	$\cdots$	$d+1-d_{h1k}$	$\cdots$	$d+1-d_{h2k}$	$\cdots$	d	$d+1$
x_1		$\cdots$		$\cdots$		$\cdots$		$\cdots$		
$\vdots$										
x_i	$\times$	$\cdots$	a_i	$\cdots$	$\times$	$\cdots$	$\times$	$\cdots$	$\times$	$\times$
$\vdots$										
x_h	$\times$	$\cdots$	$\times$	$\cdots$	a_{h1}	$\cdots$	a_{h2}	$\cdots$	$\times$	$\times$
$\vdots$										
x_m		$\cdots$		$\cdots$		$\cdots$		$\cdots$		
y_1	b_1	$\cdots$	b_1	$\cdots$	b_1	$\cdots$	b_1	$\cdots$	b_1	b_1
$\vdots$	$\vdots$		$\vdots$		$\vdots$		$\vdots$		$\vdots$	$\vdots$
y_p	b_p	$\cdots$	b_p	$\cdots$	b_p	$\cdots$	b_p	$\cdots$	b_p	b_p
$\vdots$	$\vdots$		$\vdots$		$\vdots$		$\vdots$		$\vdots$	$\vdots$
y_l	b_l	$\cdots$	b_l	$\cdots$	b_l	$\cdots$	b_l	$\cdots$	b_l	b_l

be each sequential depth. As x_{ij} $(j = 1, 2, \ldots, n)$ are separable, d_{ijk} $(j = 1, 2, \ldots, n)$ are entirely different sequential depths. Therefore, clock cycle $d+1-d_{ijk}$ $(j = 1, 2, \ldots, n)$ are entirely different and assign the values in n places of clock cycles in test sequence T_K. That is, assign the value of each primary input x_{ij} $(j = 1, 2, \ldots, n)$ in test pattern T_C to the vlaue of primary input x_i in test sequence T_K during clock cycle $d+1-d_{ijk}$ $(j = 1, 2, \ldots, n)$.

(2) Determining the values of pseudo input y_p $(p = 1, 2, \ldots, l)$

All pseudo inputs y_p $(p = 1, 2, \ldots, l)$ are not separable inputs. Therefore the sequential depth from each y_p to z_k is uniquely determined. Assign the value of pseudo input y_p in test pattern T_C to the vlaue of pseudo input y_p in test sequence T_K during clock cycle $d+1-d_{ypk}$. Taking account of making the test sequence for S_{DFT} later, assign the value of pseudo input y_p during clock cycle $d+1-d_{ypk}$ to the one except during clock cycle $d+1-d_{ypk}$. As a result, the values of pseudo inputs y_p $(p = 1, 2, \ldots, l)$ in S_K during any clock cycles are the same as the value of pseudo inputs y_p in test pattern T_C.

As mentioned above, primary inputs and primary outputs in T_K during clock cycle 1, 2, …, d, $d+1$ are determined. Let X_t and Y_t be the primary input vector and the pseudo input vector during clock cycle t, respectively. The test sequence for a fault f_K in S_K is composed of the primary input vector $[X_1, X_2, \ldots, X_d, X_{d+1}]$ and the pseudo input vector $[Y_1, Y_2, \ldots, Y_d, Y_{d+1}]$ $(Y_1 = Y_2 = \cdots = Y_d = Y_{d+1})$.

Procedure 3 : Test sequence in S_{DFT} Testing in S_K consists of assigning each input vector to the corresponding clock cycle and observing the response during clock cycle $d+1$, where d is the sequential depth of S_K. Since pseudo inputs and outputs in S_K are replaced by S-FF's and B-FF's in S_{DFT}, take account of this during testing in S_{DFT}.

The test sequence T_{DFT} for the fault f_{DFT} in S_{DFT} corresponding to f_K in S_K is as follows :

1. Operate all extended scan FF's in the shift mode and scan in the pseudo input vector Y_1.

2. (a) Operate all extended scan FF's in the hold mode and all nonscan FF's in the load mode and input the primary input vectors $X_1, X_2, \ldots, X_d$ for consecutive d clock cycles.

(b) Operate all extended scan FF's in the load mode and input X_{d+1} for 1 clock cycle.

(c) Operate all extended scan FF's in the shift mode and and scan out the test result.

The above procedure is for a fault f_{DFT} in S_{DFT}. When testing for all detectable faults in S_{DFT} is carried out, the above operation 2. is repeated the number of test times. (In this case, 2.(c) scan out the test result and scan in the next test pattern simultaneously.)

As mentioned above, when S_K is an internally balanced structure, combinational test generation is carried out in $C(S_K)$ and the test pattern is transformed into the test sequence in S_{DFT}.

The above procedure for test sequences from 1 to 3 and Theorem 3 lead to the next theorem.

Theorem 2 : Let S_K be a sequential circuit with internally balanced structure. If a fault f_K in S_K is redundant, the fault f_C in $C(S_K)$ corresponding to f_K is decided to be redundant by procedure 1. If a fault f_K in S_K is testable, the test sequnece T_K and T_{DFT} obtained by procedure 2 and 3 are the test sequences for the corresponding faults f_K in S_K and f_{DFT} in S_{DFT}, respectively. □

In order to explain that Theorem 2 is valid for internal faults in S_{DFT}, it is required to show the next theorem.

Theorem 3 : Let S_K be a sequential circuit with internally balanced structure and let each extended scan FF in S_{DFT} have the hold mode. Then a fault f_K in S_K is testable in S_K if and only if the corresponding fault f_{DFT} (an internal fault) in S_{DFT} is testable in S_{DFT}. □

(Proof) The proof of the necessary condition is evident from the above procedure transforming the test sequence.

TABLE III
EXPERIMENTAL RESULTS

Circuit	Circuit Characteristics				Area overhead				
					GGB[6]	Method 1	Method 2		
	Gates	Inputs	Outputs	FF's			FF's	Wires	Total
s1196	388	14	14	18	16	16	16	0	16
s1238	428	14	14	18	16	16	16	0	16
s1423	490	17	5	74	72	72	72	0	72
s5378	1004	35	49	179	124	124	124	0	124
s9234	2027	19	22	228	210	210	210	0	210
s9234.1	2027	36	39	211	193	193	193	0	193
s13207	2573	31	121	669	471	471	409	10	449
s13207.1	2573	62	152	638	441	441	379	10	419
s15850	3448	14	87	597	555	552	552	0	552
s15850.1	3448	77	150	534	483	480	480	0	480
s38417	8709	28	106	1636	1255	1255	1240	3	1252
s38584	11448	12	278	1452	1445	1445	1445	0	1445
s38584.1	11448	38	304	1426	1419	1419	1419	0	1419
s35932	12204	35	320	1728	1728	1704	1704	0	1704

The sufficient condition can be simply proved by partitioning S_{DFT} into the kernel circuit and the remaining circuit, and explaining that testing for a fault f_{DFT} in the kernel circuit of S_{DFT} is one for the corresponding fault f_K in S_K. For further details, refer to [13].

B. Testing for External Faults

For external faults (faults of extended scan FF's) in S_{DFT}, the following theorem holds.

Theorem 4 : Let S_{DFT} be a circuit with extended partial scan design such that the kernel circuit is an internally balanced structure. Then all irredundant faults of S-FF and B-FF in S_{DFT} are testable. □

The proof of the theorem and the details of the test sequences are omitted here due to limitations of space. For further details, refer to [13].

VIII. EXPERIMENTAL RESULTS

Using the techniques in Section VI, the experiment finding external FF's and external wires such that the kernel circuit is an internally balanced structure is carried out for ISCAS'89 benchmark circuits. Let k_1 be the hardware overhead due to replacing a FF by a S-FF and let k_2 be the hardware overhead due to replacing a wire by a B-FF. Here we assumed $k_1 : k_2 = 1 : 4$. The experimental results are shown in Table III. In Table III, *GGB* refers to the area overhead (the number of scan FF's) for the partial scan design such that the kernel circuit is a balanced structure [6]. *Method 1* refers to the area overhead (the same) for internally balanced partial scan design. *Method 2* refers to the area overhead (where *FF's* and *Wires* refers to the number of external FF's and external wires, respectively) for internally balanced extended partial scan design. From the result in Table III, s15850, s15850.1 and s35932 show that Method 1 can be implemented with low area overhead compared to GGB[6] by the effect of separating primary inputs. Moreover, s13207, s13207.1 and s38417 show that Method 2 can be implemented with the least area overhead among three methods by the effect selecting wires. However the other circuits have the same results as GGB. On the whole, Method 1 has better results than GGB and Method 2 has better results than Method 1.

IX. CONCLUSIONS

We have considered internally balanced strucure as a sequential circuit capable of combinational test generation. We have presented a method of partial scan design and extended partial scan design such that the kernel circuit is an internally balanced structure and explained their properties. Compared to partial scan design scanning only FF's, extended partial scan design has more freedom to select scan elements by selecting wires and hence low area overhead is expected for its implemetation. We have considered an algorithm for finding a set of external FF's and external wires in order to minimize the area overhead for extended partial scan such that the kernel circuit is an internally balanced structure. Moreover, for the circuit with partial scan design and extended partial scan design such that the kernel circuit is an internally balanced structure, we have presented the test procedures using the scan path and showed that those test sequences can be transformed from test patterns generated by a combinational test generation algorithm. Finally, experimental results for ISCAS'89 benchmark circuits have showed that the proposed partial scan design and extended partial scan design can be implemented with low area overhead.

Acknowledgements

The authors would like to thank Prof. Toshimitsu Masuzawa and Dr. Michiko Inoue for their comments.

This work is supported in part by the Ministry of Education of Japan under Foundation Grant 09480054.

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