Test Generation Complexity for Stuck-At and Path Delay Faults Based on τ^k-Notation

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Abstract This paper introduces τ^k-notation to be used to analyze the test generation complexity of a class of circuits with a type of faults. In this paper, we discuss classes of sequential circuits and combinational circuits with stuck-at and path delay faults, which are representative faults in logical and timing faults respectively. Using τ^k-notation, we reconsider the test generation complexity for acyclic sequential circuits with stuck-at faults. We also analyze the test generation complexity for combinational circuits and acyclic sequential circuits with robust and non-robust path delay faults. On the other hand, we define easily testable classes of cyclic sequential circuits in the aspects of the number of time frames and running time taken by the state justification and differentiation, and also the state validity for both cases of stuck-at faults and path delay faults. We also introduce two classes of cyclic sequential circuits, namely two-column state-shiftable finite state machine realizations with observable shifting logic (2COS-SSFSM) and two-column distributive state-shiftable finite state machine realizations (2CD-SSFSM). Then, we discuss the test generation complexity for these two classes with stuck-at and path delay faults. The application based on the classification of sequential circuits is two-fold. Firstly, we can apply the test generation method for combinational circuits with stuck-at faults, which is more efficient, in order to solve the test generation for each class with a type of faults. Secondly, a design for testability (DFT) or a synthesis for testability (SFT) method can be introduced based on the properties defined for each class of sequential circuits. Besides clarifying the test generation complexity, we also compare the test generation complexity for different classes of circuits with different type of faults.
keywords: τ^k-notation, easily testable, stuck-at faults, path delay faults, test generation complexity.

1 Introduction

It has been known for about three decades that the test generation problem, even for combinational circuits with stuck-at faults, is NP-complete. There does not exist an algorithm that solves an arbitrary instance of the problem in polynomial time, unless $P = NP$ is proved. However, the empirical observation showed that the test generation complexity for practically encountered combinational circuits with single stuck-at faults seems to be polynomial. Based on this observation, the works related to the classification of sequential circuits started.

Several classes of acyclic sequential circuits have been introduced in the previous works. These include balanced sequential circuits, internally balanced sequential circuits and so on. The test generation for internally balanced sequential circuits and balanced sequential circuits with stuck-at

faults has been shown to be reducible into that for combinational circuits with stuck-at faults[1,2]. The test generation complexity for acyclic sequential circuits has not yet been clarified. Neither has been that for cyclic sequential circuits. Apart from stuck-at fault, which is the representative fault of static faults, path delay fault model, which is the most powerful timing fault model, is important to ensure the temporal correctness of a circuit. Therefore, we include path delay faults in our discussion. As the first step of the work, we consider only robust and non-robust faults in this paper. The relationships between the test generation for combinational circuits with path delay faults and that with stuck-at faults have been discussed in [3,4,5,6]. They showed that the ATPG for stuck-at faults plus some polynomial circuit transformations can be used as an ATPG for robust and non-robust path delay faults. The test generation was not discussed explicitly in the aspect of time complexity. Neither was the test generation complexity for sequential circuits with path delay faults.

When more and more classes of circuits are introduced and the discussion of the test generation complexity for each class with different type of faults becomes important, it would be helpful if there is a general notation to be used in the discussion. Therefore, we introduce τ^k-notation prior to the discussion of the test generation complexity. By using τ^k-notation, we reconsider the test generation complexity for balanced sequential circuits[2] and internally balanced sequential circuits[1] with stuck-at faults, which is reducible to the test generation for combinational circuits with stuck-at faults. We also review the test generation complexity for combinational circuits with robust and non-robust path delay faults, which is also equivalent to the test generation for combinational circuit with stuck-at faults. Besides, we analyze the test generation complexity for sequential circuits including cyclic sequential circuits with stuck-at and path delay faults. Clarifying the test generation complexity for several classes of sequential circuits with faults leads to two applications. First, based on the properties of a known class, a special ATPG is designed to run the test generation on the circuit, which is generally more efficient than does the general sequential ATPG. For instance, the test generation technique involving separating of separable inputs, wire replacing and combinational test generation and sequence transformation, is used to obtain a test in an internally balanced sequential circuits, the test generation time of which has been proved reduced[1]. Another application is design for testability (DFT) and synthesis for testability (SFT). For example, based on the feature of balanced structure, the DFT called BALLAST was introduced[2]. For a given arbitrary sequential circuit (resp. arbitrary design), a DFT method (resp. SFT method) is designed and applied to augment the circuit into one of the easily testable classes of sequential circuits.

After clarifying the test generation complexity for each class of circuits with stuck-at and path delay faults, our concern is to compare the test generation complexity for stuck-at faults and that for path delay faults. We have obtained they are equivalent for combinational circuits, balanced sequential circuits, and internally balanced sequential circuits. For acyclic sequential circuits, they are equivalent under time expansion model (TEM)[7] at slow-fast-slow clock but still it is unknown at rated clock. For cyclic sequential circuits, they are equivalent for l-length-bounded testable circuits, l-length-bounded validity-identifiable circuits, t-time-bounded testable circuits and t-time-bounded validity-identifiable circuits, and two-column SSFSM realization with observable shifting logic. Then our interest is whether there exists any class of circuits, the test generation complexities for which with stuck-at faults and path delay faults are not equivalent. If there exists such class of circuits, the following question arises. "Which complexity is higher, the one for stuck-at faults or path delay faults?" We have shown there is a class of sequential circuits named two-column distributive SSFSM realizations, the test generation for stuck-at faults and that for path delay faults of which might not be equivalent; by showing in a conjecture that its test generation for path delay faults might have less complexity than its test generation for stuck-at faults.

The organization of the rest of the paper is as follows. In Section 2, we briefly review the definitions of fault models and define τ^k-notation. In Section 3, we reconsider the test generation complexity for combinational circuits with robust and non-robust path delay faults. We also consider the test generation complexity for combinational circuits with robust and non-robust segment delay faults in Section 4 as the result is useful in analyzing the test generation complexity for sequential circuits with path-delay faults. In Section 5, we discuss the test generation complexity for acyclic sequential circuits with stuck-at and path delay faults. This is followed by the discussion of the test generation complexity for several classes of cyclic sequential circuits with stuck-at and path delay faults in Section 6. Conclusion is presented in the final section.

2 Preliminaries

Before discussing the test generation complexity for several classes of circuits with stuck-at faults and path delay faults, the definitions related to the fault models and τ^k-notation are briefly reviewed in this section.

2.1 Fault Models

Testing of logical faults is necessary to make sure that the interconnections in a given circuit are fault-free and are able to carry both logic 0 and 1 signal. The logical fault model detects defects which occur independent of the speed. Therefore, the testing of logical faults is also called static testing. The most popular fault model for digital circuits is stuck-at fault model. The single stuck-at fault models several possible physical faults; moreover, the stuck-at fault model is easily manageable by algorithms.

A fault may also affect the circuit's temporal behavior; such faults are called timing faults or dynamic faults. Timing faults are modeled as an increase in the propagation time of a gate. As the increasing emphasis on designing the circuits for very high performance taking place, timing test becomes more and more important to ensure the temporal correctness of a circuit. The most realistic model for timing faults is path delay fault model.

In a sequential circuit, a path is defined as an ordered set of gates $\{g_1, g_2, ..., g_m\}$, where g_1 is a primary input or a flip-flop and g_m is a primary output or a flip-flop. Also, gate g_i is an input to gate g_{i+1} $(1 \leq i \leq m-1)$. A path has a delay fault if for any input sequence that generates a rising or falling transition through the path, the propagation time of such transition exceeds a specified clock period. Such a delay fault on a path is said to be a *path delay fault* (PDF). Let $\mathcal{S}$ denote a sequential circuit and P denote a path in $\mathcal{S}$. Let f be a rising (resp. falling) PDF on P and let $\mathcal{S}_f$ be the faulty circuit of $\mathcal{S}$ in the presence of f. The fault is also denoted by $P\uparrow$ (resp. $P\downarrow$). The fault f is *testable* if there exists an input sequence t for $\mathcal{S}$ and $\mathcal{S}_f$ such that the following conditions hold.

C1. A rising (resp. falling) signal transition is launched at the starting point (a flip-flop or a primary input) of P in $\mathcal{S}$ by t.

C2. The transition launched at the starting point of P is propagated to the ending point (a flip-flop or a primary input) of P along P in $\mathcal{S}$ by t.

C3. The captured or observed value induced by the transition at the ending point of P in $\mathcal{S}_f$ is different from that of $\mathcal{S}$.

C4. The output sequence of $\mathcal{S}$ and that of $\mathcal{S}_f$ are different.

Such an input sequence t is regarded as a *PDF test sequence*. As the first step of our work, we consider only robust and non-robust path delay faults besides stuck-at faults.

2.2 Test Generation Complexity for Combinational Circuits with Single Stuck-At Faults

It has been known theoretically for about three decades that the test generation complexity is NP-complete, even for combinational circuits with single stuck-at faults. However, practically it seems to be polynomial. Thanks to this empirical observation, we can discuss the test generation complexity for several classes of circuits with a type of faults. Therefore, we have the following assumption for our discussion.

Assumption: The test generation complexity for combinational circuits with stuck-at faults is $\Theta(n^r)$ for some r larger than 2, where n is the size of a combinational circuit.

2.3 τ^k-Notation

To clarify the test generation complexity for several classes of circuits with stuck-at and path delay faults and to compare the relationships between the test generation problems, we introduce τ^k-notation.

P_C^F: **Test Generation Problem for Combinational Circuits C with Faults of Type F**

Instance: A combinational circuit $c \in C$ and a fault $f \in F$.
Question: Is there a test pattern to detect f in c?

P_S^F: **Test Generation Problem for Sequential Circuits S with Faults of Type F**

Instance: A sequential circuit $s \in S$ and a fault $f \in F$.
Question: Is there a test sequence to detect f in s?

P_α^F: **Test Generation Problem for Class α with Faults of Type F**

Instance: A sequential circuit $s \in \alpha$ and a fault $f \in F$.
Question: Is there a test sequence to detect f in s?

Definition 2.1. *The time complexity of a problem P is the time complexity of the fastest algorithm for the problem P. Let P_C^F, P_S^F and P_α^F be the test generation problem for class C, class S and class α, respectively with faults of type F. Let $T_C^F(n), T_S^F(n)$ and $T_\alpha^F(n)$ be the time complexity of P_C^F, P_S^F and P_α^F, respectively where n is the size of the problem instance. $T_C^F(n), T_S^F(n)$ and $T_\alpha^F(n)$ is also called test generation complexity for class C, class S and class α, respectively with faults of type F.*

Let $T_C^{sSA}(n)$ denote the test generation complexity for combinational circuits with single stuck-at faults. We consider $T_C^{sSA}(n)$ as a basic unit of the time complexity of the test generation problem. And, $\tau(n)$ is used to denote $T_C^{sSA}(n)$ in the following text, where $\tau(n) = T_C^{sSA}(n) = \Theta(n^r)$ for some constant $r \geq 2$, where n is the size of the problem instance.

Definition 2.2. *$T(n)$ is τ^k-equivalent if and only if $T(n) = \Theta(\tau^k(n))$ and τ^k-bounded if and only if $T(n) = O(\tau^k(n))$, where $k > 0$.*

Definition 2.3. *Class α with faults of type F is τ^k-equivalent if and only if $T_\alpha^F(n) = \Theta(\tau^k(n))$ and τ^k-bounded if and only if $T_\alpha^F(n) = O(\tau^k(n))$, where $k > 0$.*

3 Test Generation Complexity for Combinational Circuits with Path Delay Faults

As mentioned in the previous section, we assume that the test generation complexity for combinational circuits with stuck-at faults is $\Theta(n^r)$ for some constant r larger than 2 and it is denoted by $\tau(n)$. In this section, we consider the test generation complexity for combinational circuits with robust and non-robust path delay faults based on τ^k-notation.

A full leaf-dag is a combinational circuit such that a fanout and an inverter are only permitted at the primary inputs and the output of an inverter is not allowed to have a fanout [3]. We define a single-path leaf-dag C_P^{LD} for path P and a path rising-smooth circuit C_P^{RS} based on [3] in order to facilitate the following discussion.

Definition 3.1. *A single-path leaf-dag C_P^{LD} for path P is a combinational circuit such that a fanout and an inverter along P are only permitted at the starting point of P and the output of the inverter, if one exists along P, is not allowed to have fanouts.*

Definition 3.2. *Let P denote a path in a given combinational circuit C. C can be transformed into a single-path leaf-dag C_P^{LD} for path P, by the single-path-leaf-transformation:*

S1. P consists of an ordered set of gates $\{g_1, g_2, ..., g_m\}$, where g_1 is a primary input and g_m is a primary output. Also, gate g_j is an input to gate g_{j+1} $(1 \leq j \leq m-1)$. Let $Pre(g_j)$ denote a set of predecessor gates $\{g_1, g_2, ..., g_{j-1}\}$ on P. Traversing from g_m, if a gate g_j has a fanout of two or more, each gate in $Pre(g_j)$ with the connections to its immediate predecessor gates are duplicated once. Let g'_k denote the duplicate of g_k, where $g_k \in Pre(g_j)$. For each g_k in $Pre(g_j)$ and for each immediate successor gate h_{k+1} of g_k which is not on P, the connection of g_k to h_{k+1} is changed to the connection of g'_k to h_{k+1}. The resulting path P is free of fanout.

S2. Starting from g_m along P, all the NAND (resp. NOR) gates on P are changed to the OR (resp. AND) gates using De Morgan's Law.

Let n denote the number of gates of a given combinational circuit. Let n_p and n'_p denote the number of gates along P and the number of gates along P that are duplicated. Note that the size of the resulting circuit after this transformations is $n' = n + n'_p$. Since $n'_p \leq n_p \leq n$, the size of the transformed circuit is at most $2n$.

Definition 3.3. *The I-edge of path P with input i in a single-path leaf-dag C_P^{LD} refers to the first connection of P after the inverter, if it exists. The I-edge is said to be associated with input i.*

Definition 3.4. *A single-path leaf-dag C_P^{LD} for path P can be transformed into a path rising-smooth circuit C_P^{RS} (resp. path falling-smooth circuit C_P^{FS}) for path P by the path rising-smooth (resp. path falling-smooth) transformation:*

S1. Let Q_{OR} (resp. Q_{AND}) denote the OR gates (resp. AND gates) along P that have a rising (resp. falling) transition along. A gate may have no parity, 0, 1 or both parities. A gate fed to the side-input of an OR gate (resp. AND gate) in Q_{OR} (resp. Q_{AND}) has parity 1 (resp. 0). Perform a reverse topological traversal of the gates Q in the transitive fanout of i, to determine the parity of all gates along the side-paths to P where i is the primary input on P. The parity is complemented across a NOT gate. If some fanouts of a gate have parity 1 and others have parity 0, the gate is assigned both parities.

S2 Duplicate the gates so that each resulting gate is either nothing, 0, or 1, but not both, depending on its successor gates.

S2.1 Traversing from the primary output g_m on P, for each gate h_j with a parity (parities) and with a successor gate that is off path and without parity, h_j and the connections to its immediate predecessor gates are duplicated once and its duplicate h'_j has no parity. For each immediate successor gate h_{j+1} of h_j that is off path and has no parity, the connection from h_j to h_{j+1} is replaced by the connection from h'_j to h_{j+1}.

S2.2 Traversing from the primary output g_m on P, each gate h_j with both parities and the connections to its immediate predecessor gates are duplicated once and assigned parity 1. Its duplicate h'_j is assigned parity 0. For each immediate successor gate h_{j+1} of h_j that has parity 0 (1 if there is an inversion between h_j and h_{j+1}), the connection from h_j to h_{j+1} is replaced by the connection from h'_j to h_{j+1}.

S3. Let input i denote the primary input on P. Assign 0 to any fanout branch of input i (or the first connection after the inverter, if it exists on the fanout branch) that is connected to a gate with parity 0 and 1 to any fanout branch of input i (or the first connection after the inverter, if it exists on the fanout branch) that is connected to a gate with parity 1.

Let n denote the number of gates of a given combinational circuit. Note that the size of the resulting circuit after the single-path-leaf transformation is $n' = n + n'_p$ where $n'_p \leq n_p \leq n$. During the path rising-smooth transformation on this circuit with size n', the gates that are potential to be duplicated are gates other than those on P and their duplicates, the number of which is $n' - n_p - n'_p$. Therefore, the size of the resulting circuit is $n'' = 2n' - n_p - n'_p = 2n + n'_p - n_p$ for $n' = n + n'_p$. The size of the resulting circuit is at most $2n$ because the maximum value of $n'_p - n_p$ is 0 where $n'_p \leq n_p$.

Example Figure 1 shows a combinational circuit(a), its full leaf-dag and rising smooth circuit, and its single-path leaf-dag and path rising-smooth circuit for $c2367x$. Gate 1 is duplicated once while gate 2 is duplicated twice in the transformation to a rising-smooth circuit (Figure 1(b)). Whereas, only gate 2 is duplicated twice in transforming the circuit into a path rising-smooth circuit shown in Figure 1(c).

Definition 3.5. [5] *A vector pair $< \tilde{v}, v >$ is a single-input-change (SIC) two-pattern test if there exists a coordinate i such that $\tilde{v}_i = \overline{v}_i$ for the coordinate i of v and $\tilde{v}_j = v_j$ for each coordinate j other than i.*

Lemma 3.1. *Let C denote a given combinational circuit with size n and $P\uparrow$ (resp. $P\downarrow$) denote a rising (resp. falling) path delay fault(PDF). The time complexity of the single-path-leaf transformation on C with $P\uparrow$ (resp. $P\downarrow$) is $O(n^2)$.*

Proof. Let the `SuccessorGate of G` denote an immediate successor gate of `G`. Let the `PredecessorGates` denote all immediate predecessor gates of `G`. Let PI and PO denote primary input and primary output respectively. The following shows the pseudocode for the single-path-leaf transformation.

```
Single-path-leaf transformation (C, P)
FOR each G on P from the PO //n+1 times
  IF G has a fanout of more than one
    SET FirstFanout as G
    BREAK LOOP FOR
```

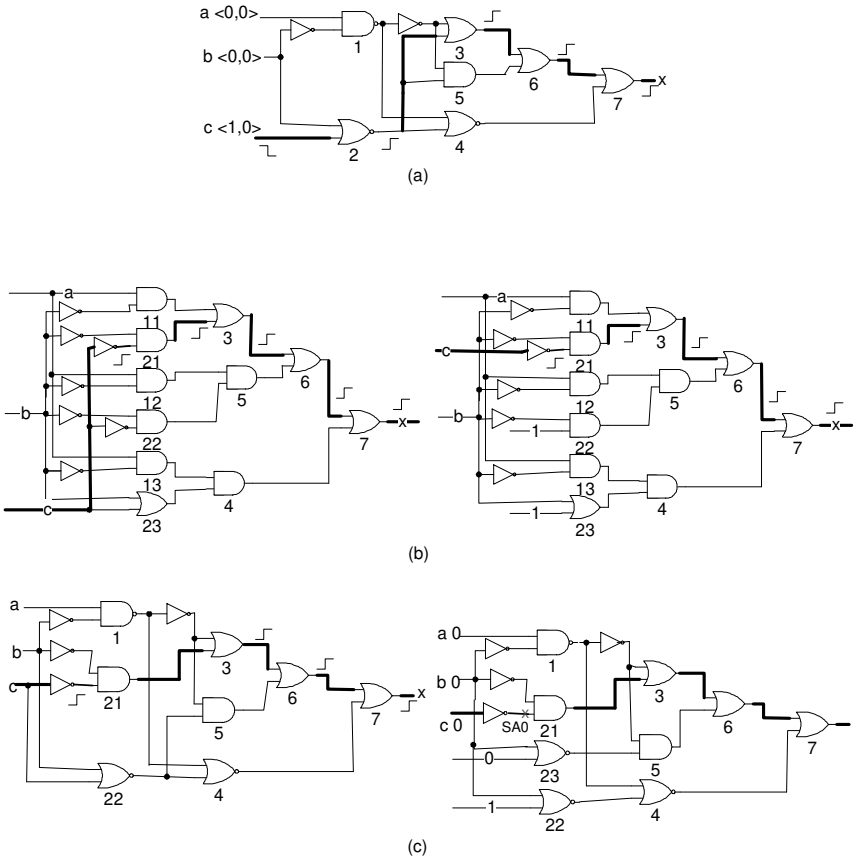

Figure 1: (a) A PDF $c2367x \uparrow$. (b) A full leaf-dag (left) and a rising-smooth circuit (right) (c) A single-path leaf-dag (left) and a path rising-smooth circuit (right).

```
 END IF
END FOR

FOR each G on P from FirstFanout to the PI //n+1 times
  duplicate G as G'
  connect G' to PredecessorGates
  FOR each SuccessorGate of G //n*n times
    IF SuccessorGate is not on P THEN
      Replace connection G to SuccessorGate by connection G' to SuccessorGate
    END IF
  END FOR
END FOR

FOR each G on P from the PO to the PI //n+1 times
  Change NAND gates and NOR gates to AND gates and OR gates, respectively
END FOR
```

The pseudocode proves the lemma. The proof for $P\downarrow$ can be derived similarly. □

Lemma 3.2. *Let C denote a single-path leaf-dag with size n and $P\uparrow$ (resp. $P\downarrow$) denote a rising (resp. falling) PDF. The time complexity of the path rising-smooth (resp. path falling-smooth) transformation on C with $P\uparrow$ (resp. $P\downarrow$) is $O(n^2)$.*

Proof. The proof is only for $P\uparrow$. The similar proof can be derived for $P\downarrow$ by considering AND gates instead of OR gates and all the parity in the pseudocode below is complemented. Let g denote the number of the OR gates on P while h denote the total number of gates on P and their duplicates where $g, h \leq n$. Let `SuccessorGate of G` and `PredecessorGates` denote an immediate successor gate and all immediate predecessor gates, respectively of `G` and i denote the primary input on P. Let PI and PO denote primary input and primary output respectively. The following pseudocode proves the lemma.

```
Path rising-smooth transformation (C, P)
 FOR the G at the side-input of each ORGate on P from PO to PI //g+1 times
   IF there's an inversion between G and ORGate THEN
     Assign to G a parity 0
   ELSE
     Assign to G a parity 1
   END IF
 END FOR

 FOR each G from PO on P in the transitive fanout of PI i on P //n+1 times
   FOR each SuccessorGate of G //n*n times
     IF there is an inversion between G and SuccessorGate THEN
       Assign to G a parity complemented to the SuccessorGate's
     ELSE
       Assign to G a parity same as SuccessorGate's
     END IF
   END FOR
```

```
END FOR

FOR each G with a parity //n-h+1 times
  IF there's an offpath SuccessorGate without parity THEN
    Duplicate G as G'
    Connect G' to PredecessorGates
    FOR each offpath SuccessorGate of G //(n-h)*(n-h) times
      IF SuccessorGate has no parity
        Replace connection from G to SuccessorGate
        by connection from G' to SuccessorGate
      END IF
    END FOR
  END IF
END FOR
FOR each G with both parities //n-h+1 times
  Duplicate G as G'
  Connect G' to PredecessorGates
  Assign to G a parity 1
  Assign to G' a parity 0
  FOR each SuccessorGate //(n-h)*(n-h) times
    IF the parity is 0
    (1 if there is an inversion between G and SuccessorGate) THEN
      Replace the connection from G to SuccessorGate
      by a connection from G' to SuccessorGate
    END IF
  END FOR
END FOR

FOR each G connected to i //2n times
  Assign to G 1 if the parity is 1
  Assign to G 0 if the parity is 0
END FOR
```

□

Lemma 3.3. *The time complexity of SIC two-pattern n-bit test transformation is $O(n)$.*

Proof. Let v denote a test obtained from a test generation. The first pattern $\tilde{v}$ can be derived by complementing the value v_i for $\tilde{v}_i$ and duplicate other v_j for $\tilde{v}_j$, where $i \neq j$ based on the definition of SIC, which can be done in linear time. □

Definition 3.6. *A fanout-inverter-free single-path leaf-dag C_{FP}^{LD} for path P is a single-output single-path leaf-dag C_P^{LD} for path P that satisfies the following conditions:*

C1. P consists of an AND gate and does not have fanout and inverter.

C2. There exists a transitive fanin cone of c that is the side-input of AND gate along P.

Figure 2 shows the fanout-inverter-free single-path leaf-dag. Let $\boldsymbol{C_P^{LD}}$, $\boldsymbol{C_P^{RS}}$ and $\boldsymbol{C_{FP}^{LD}}$ denote the classes of single-path leaf-dags, path rising-smooth circuits and fanout-inverter-free single-path

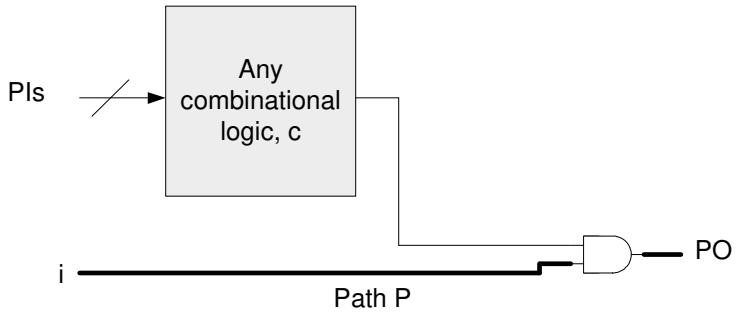

Figure 2: A fanout-inverter-free single-path leaf-dag.

leaf-dags for path P, respectively. Based on Definitions 3.2 and 3.4, $\boldsymbol{C_{FP}^{LD} \subset C_{P}^{LD}}$ and $\boldsymbol{C_{FP}^{LD} \subset C_{P}^{RS}}$. Note that the transitive fanin of c can be any combinational logic. It is well-known that the combinational test generation problem for combinational circuit C with stuck-at faults is polynomially transformable into CIRCUIT-SAT(C') problem where C' is an XOR function of circuit C and its faulty circuit C_f. It is obvious that CIRCUIT-SAT(C') problem can be transformed polynomially into the test generation for fanout-inverter-free single-path leaf-dags $\boldsymbol{C_{FP}^{LD}}$ for path P with robust PDFs at path P where $c = C'$.

Lemma 3.4. *v is a test for a SAF f in C if and only if $< v+0, v+1 >$ (resp. $< v+1, v+0 >$) is a robust test for the $P\uparrow$ (resp. $P\downarrow$) in the corresponding fanout-inverter-free single-path leaf-dag C_{FP}^{LD} for P with $c = C \oplus C_f$ where $v + b$ means the concatenation of vector v and bit b that is a value at the primary input of P.*

Proof. **If part:** $< v + 0, v + 1 >$ is a robust test for the $P\uparrow$ in a fanout-inverter-free single-path leaf-dag C_{FP}^{LD} with $c = C \oplus C_f$. The partial two-pattern vector $< 0, 1 >$ launches the $P\uparrow$ while the partial two-pattern vector $< v, v >$ generates the stable non-controlling values at the side-input of AND gate on P. This means $c = C \oplus C_f$ has a stable value 1 under $< v + 0, v + 1 >$. Therefore, v is a test for SAF f in C.
Only if part: v is a test for SAF f in C. v generates 1 at c as c is a boolean circuit casting the CIRCUIT-SAT problem that is equivalent to the test generation problem of SAF f. By applying $< v, v >$ to the partial circuit c, stable non-controlling values are generated at the side-input of AND gate on P. Therefore, $< v + 0, v + 1 >$ is also a robust test for the $P\uparrow$. □

Lemma 3.5. *The test generation complexity for fanout-inverter-free single-path leaf-dags for path P with robust PDFs at path P is equivalent to the test generation for combinational circuits with SAFs, which is τ-equivalent.*

Proof. Lemma 3.4 proved the equivalence of test generation problems for fanout-inverter-free single-path leaf-dags with PDFs and combinational circuits with SAFs, where combinational circuits with SAFs is assumed τ-equivalent. □

Lemma 3.4 and 3.5 will be used as part of the proofs of the test generation complexity for PDFs and SDFs in this section and the following section.

Lemma 3.6. *The test generation complexity for combinational circuits with SAFs at primary inputs is τ-equivalent.*

Proof. In the beginning of the paper, combinational circuits with SAFs is assumed τ-equivalent. According to the definition of I-edge, a primary input is a special case of I-edge. And, Lemma 3.5 shows that the test generation complexity for a subclass of combinational circuits with SAFs at I-edges is τ-equivalent. Lemma 3.6 is proved. □

3.1 Test Generation Complexity for Robust Path Delay Faults

This section discusses the test generation complexity for combinational circuits with robust path delay faults.

Lemma 3.7. [3] $< v_1, v_2 >$ *is a robust test for the* $P \uparrow$ *(resp.* $P \downarrow$*) in the path rising-smooth-circuit* C_P^{RS} *for* P*, if and only if* $< v_1, v_2 >$ *is a robust test for the* $P \uparrow$ *(resp.* $P \downarrow$*) in the single-path leaf-dag* C_P^{LD} *for* P*.*

Proof. The following is the proof for the case of $P \uparrow$. The proof for the case of $P \downarrow$ can be done analogously by considering AND gates instead of OR gates. Let i be the input of P. Let P_I denote the side-paths to OR gates along P in C_P^{LD}, such that the I-edge of each $Q \in P_I$ is associated with input i.
If part: $< v_1, v_2 >$ is a robust test for the $P \uparrow$ in C_P^{LD}. By the definition of robust test, each side-input along path $Q \in P_I$ to an OR gate along P in C_P^{LD} is at a steady non-controlling value (0) value with no transitions although there is a transition at the I-edge of each $Q \in P_I$ associated with i on the application of v_2 after v_1. This implies that asserting any constant value at the I-edge of each $Q \in P_I$ in C_P^{RS} leaves the value on these side-inputs unchanged under $< v_1, v_2 >$. Hence $< v_1, v_2 >$ remains a test for P in C_P^{RS}.
Only if part: Only the I-edges of paths in P_I are set to 1 or 0 according to their parities in obtaining C_P^{RS} from C_P^{LD}. By the definition of robust test, each side-input to OR gates along P in C_P^{RS} is at a steady non-controlling(0) value. This implies that the constants 1 or 0 asserted at the I-edge of each path in P_I according to their parities does not propagate to the side-inputs of these OR gates. Otherwise, the side-inputs to the OR gates are not guaranteed to be at non-controlling value under v_2. In other words, none of the transitions at the corresponding I-edges in C_P^{LD} propagate to the side-inputs of OR gates along P. Since the side-inputs of all other gates along P are same in C_P^{LD} and C_P^{RS}, $< v_1, v_2 >$ is a robust test for P in C_P^{LD}. □

Lemma 3.8. [3] v *is a test for the SA0(resp. SA1) fault at the I-edge of* P *in the* C_P^{RS} *for path* P *if and only if the SIC vector* $< \tilde{v}, v >$ *is a robust test for the* $P \uparrow (P \downarrow)$ *in* C_P^{LD}*.*

Proof. **If part:** Let $< \tilde{v}, v >$ be a robust test for the $P \uparrow$ in C_P^{LD}. Then it is also a robust test for the $P \uparrow$ in C_P^{RS} according to Lemma 3.7. The output P is 1 when v is applied to the C_P^{RS} for P. Consider what happens in the presence of the SA0 fault at the I-edge of P in C_P^{RS} under vector v. By the definition of robust test, each side-input to the OR gates on P is at a non-controlling value under v. The I-edge of P is 1 (in the absence of the fault) under vector v in C_P^{RS}. Hence v is a test for the SA0 fault at the I-edge of P in C_P^{RS}.
Only if part: Let v be a test vector for the SA0 fault at the I-edge of P in the C_P^{RS} for P. i is the only input in C_P^{RS} that changes under the vector pair $< \tilde{v}, v >$. Let P_S denote the side-paths to P whose I-edges are not associated with i. Each side-input to P that belongs to a side path in P_S must be at a non-controlling value under v; this is due to the test condition for the SAF. Among the remaining side-inputs, let I_{and} denote the side inputs that meet P at an AND gate, and let I_{or} denote the side-inputs that meet P at an OR gate. I_{or} is empty by construction of the C_P^{RS} because the side-paths to OR gates on P that have i as inputs have been separated to form new inputs during the transformation. Since a SA0 fault is being tested, each side input to

P in I_{and} is at value 1 in C_P^{RS} under v (in the absence of the fault). Apply the vector $\tilde{v}$ to the circuit. The side-inputs to P in I_{and} may be at either value 0 or 1. Then, apply the vector v. The side-input to P in I_{and} may change to 1, or they may remain at 1, possibly with dynamic or static hazards, respectively. All the other side-inputs to P remain at hazard-free non-controlling values, since the transition on i under the vector pair cannot propagate to these side-inputs in the C_P^{RS}. The transition that propagates along P is a 0-to-1 transition, which propagates a delay fault at each AND gate along P irrespective of the presence of hazards on the side-inputs, provided the side-inputs have a final value of 1. Since this condition holds, $< \tilde{v}, v >$ is a robust test for the rising transition along P in C_P^{RS}, and hence in C_P^{LD}. □

Lemma 3.9. *The test generation for combinational circuits with robust PDFs and the test generation for path rising-smooth circuits with SAFs at I-edges are equivalent, which are τ-bounded.*

Proof. Lemma 3.7 and 3.8 have proved the equivalence between the test generation for combinational circuits with robust PDFs and the test generation for path rising-smooth circuits with SAFs at I-edges. Therefore, a two-pattern robust test on a combinational circuit C for $P\uparrow$ (resp. $P\downarrow$) can be performed using combinational test generation for SAFs by the following procedure.

S1. Perform the single-path-leaf transformation for P on C and the resulting circuit is C_P^{LD}.

S2. Perform the path rising-smooth transformation (resp. path falling-smooth transformation) on C_P^{LD} for P and the resulting circuit is C_P^{RS} for path P.

S3. Perform the combinational test generation for SA0 (resp. SA1) at the I-edge associated with i in C_P^{RS}. Let v denote the test.

S4. Transform v into the SIC two-pattern test $< \tilde{v}, v >$.

Let n be the size of a given combinational circuit C. Let T_{SPL}, T_{PRS}, T_C^{sSA} and T_P denote the time complexity of the single-path-leaf transformation, the time complexity of the path rising-smooth transformation, the combinational test generation for combinational circuits with single SAFs and the two-pattern transformation. Let N_{SPL}, N_{PRS}, N_C^{sSA} and N_P denote the problem sizes of the single-path-leaf transformation, the path-rising-smooth transformation, the combinational test generation for combinational circuits with single SAFs and the two-pattern transformation, respectively. According to Lemma 3.1-3.3 and for $N_{SPL} = n$, $n \leq N_{PRS} \leq 2n$, $n \leq N_C^{sSA} \leq 2n$ and $N_P \leq n$. Therefore, the test generation complexity is

$$\begin{aligned} T_C^{rPD}(n) &= T_{SPL}(N_{SPL}) + T_{PRS}(N_{PRS}) + O(T_C^{sSA}(N_C^{sSA})) + T_P(N_P) \\ &= O(N_{SPL}^2) + O(N_{PRS}^2) + O(\tau(N_C^{sSA})) + O(N_P) \\ &= O(n^2) + O(n^2) + O(\tau(2n)) + O(n) \\ &= O(\tau(n)). \end{aligned}$$

□

Theorem 3.1. *The test generation complexity for combinational circuits with robust PDFs is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

Proof. To prove that the test generation for combinational circuits with robust PDFs and the test generation for combinational circuits with SAFs are equivalent, we need to show that the test generation for combinational circuits with SAFs is equivalent to that for a subclass of path rising-smooth circuits with robust PDFs in addition to Lemma 3.9. Since fanout-inverter-free single-path leaf-dags is a subclass of single-path leaf-dags, Lemma 3.5 and Lemma 3.9 prove the theorem. □

3.2 Test Generation Complexity for Non-Robust Path Delay Faults

This section elaborates the test generation complexity for combinational circuits with non-robust path delay faults.

Lemma 3.10. *v is a test for the SA0(resp. SA1) fault at the I-edge of P in the C_P^{LD} for path P if and only if $< \tilde{v}, v >$ is a non-robust test for the $P\uparrow(P\downarrow)$ in C_P^{LD}.*

Proof. **If part:** Let $< \tilde{v}, v >$ be a non-robust test for $P\uparrow$ in C_P^{LD}. The output of P is 1 when v is applied to C_P^{LD}. Consider the case of the presence of SA0 at the I-edge of P in C_P^{LD} under vector v. From the definition of non-robust test, each side-input to P is at a non-controlling value under v. The I-edge of P is 1 under v in the absence of the fault $P\uparrow$. According to test condition, the SA0 is excited and its fault effect propagates to the output in C_P^{LD}. Hence v is a test for the SA0 fault at the I-edge of P in C_P^{LD}.
Only if part: Let v be a test vector for the SA0 at the I-edge of P in C_P^{LD}. i is the input that changes under the vector pair $< \tilde{v}, v >$. Under the test condition, the side inputs along P are at non-controlling value under v. When vector $\tilde{v}$ is applied, the side-inputs to P may be at either value 0 or 1. The side-inputs to P may change to non-controlling value or remain at non-controlling value. According to the definition of non robust test, only the second vector of side-inputs must be non-controlling value. Thus, $< \tilde{v}, v >$ is a non-robust test for $P\uparrow$ in C_P^{LD}. □

Lemma 3.11. *The test generation for combinational circuits with non-robust PDFs is equivalent to the test generation for single-path leaf dags with SAFs at I-edges, which is τ-bounded.*

Proof. Based on Lemma 3.10, the following procedure generates a two-pattern non-robust test on a combinational circuit for SAFs test generation method.

S1. Perform the single-path-leaf transformation on C with path P. The resulting circuit is called single path-leaf-dag C_P^{LD} for P.

S2. Perform the combinational test generation for SA0 (resp. SA1) at I-edge of P associated with i in C_P^{LD}. Let v denote the test.

S3. Transform v into the SIC two-pattern test $< \tilde{v}, v >$.

Let n be the size of a given combinational circuit C. Let T_{SPL}, T_C^{sSA} and T_P denote the time complexity of the single-path-leaf transformation, the combinational test generation for single SAFs and the two-pattern transformation. Let N_{SPL}, N_C^{sSA} and N_P denote the problem sizes of the single-path-leaf transformation, the combinational test generation for single SAFs and the two-pattern transformation, respectively. According to Lemma 3.1 and 3.3 and also for $N_{SPL} = n$, $n \leq N_C^{sSA} \leq 2n$ and $N_P \leq n$. Therefore, the test generation complexity is

$$\begin{aligned} T_C^{nrPD}(n) &= T_{SPL}(N_{SPL}) + O(T_C^{sSA}(N_C^{sSA})) + T_P(N_P) \\ &= O(N_{SPL}^2) + O(\tau(N_C^{sSA})) + O(N_P) \\ &= O(n^2) + O(\tau(2n)) + O(n) \\ &= O(\tau(n)). \end{aligned}$$

□

Theorem 3.2. *The test generation complexity for combinational circuits with non-robust PDFs is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

Proof. To show that the test generation for combinational circuits with PDFs and the test generation for combinational circuits with SAFs are equivalent, we need to prove that the test generation for combinational circuits with stuck-at faults is equivalent to the test generation for a subclass of single-path leaf-dags with faults of a subclass of PDF. Since fanout-inverter-free single-path leaf-dags is a subclass of single-path leaf-dags and robust PDF is a subset of non-robust PDF, Lemma 3.5 in addition to Lemma 3.11 proves the theorem. □

From Theorems 3.1 and 3.2, we can see that the combinational test generation complexity for robust and non-robust PDFs is τ-equivalent.

4 Test Generation Complexity for Combinational Circuits with Segment Delay Faults

In Section 3, we showed that the combinational test generation complexity for robust and non-robust PDFs is τ-equivalent. In this section, we consider segment delay faults (SDFs) and evaluate the test generation complexity for combinational circuits with those faults. The result will be used in Sections 5 and 6 to study the test generation complexity for acyclic sequential circuits with PDFs.

Definition 4.1. *An n-bit vector v_l consists of $(v_1^l, v_2^l, ..., v_j^l, ..., v_n^l)$.*

Definition 4.2. *A segment-leaf-dag C_S^{LD} for segment S ($S = \{g_1, g_2, ..., g_m\}$) is a combinational circuit such that a fanout and an inverter are only permitted at g_1 of the segment S and the output of an inverter along S is not allowed to have a fanout.*

Definition 4.3. *Let S denote a segment in a given combinational circuit C. C can be transformed into C_S^{LD}, by the segment-leaf transformation:*

S1. S consists of an ordered set of gates $\{g_1, g_2, ..., g_m\}$, where the output of g_1 is the starting point of S and the output of g_m is the ending point of S, respectively. Also, gate g_i is an input to gate g_{i+1} $(1 \leq i \leq m-1)$. Let $Pre(g_i)$ denote a set of gates $\{g_2, g_3, ..., g_{i-1}\}$ on S. Traversing from g_m, if a gate g_i has a fanout of two or more, each gate in $Pre(g_i)$ with the connections to its immediate predecessor gates are duplicated once. Let g_j' denote the duplicate of g_j, where $g_j \in Pre(g_i)$. For each g_j in $Pre(g_i)$ and for each immediate successor gate h_{j+1} of g_j, the connection from g_j to h_{j+1} is changed to the connection from g_j' to h_{j+1} if h_{j+1} is not on S. The resulting segment S is free of fanout.

S2. Starting from g_m along S, all the NAND (resp. NOR) gates on S are changed to the OR (resp. AND) gates using De Morgan's Law.

Note that the segment-leaf-transformation is defined analogously to the single-path-leaf transformation by considering segment S instead of path P.

Definition 4.4. *The S-edge of segment S with starting point s in a segment-leaf-dag C_S^{LD} refers to the first connection of S after the inverter, if it exists. The S-edge is said to be associated with s.*

Example Figure 3 shows a combinational circuit (a) and its segment leaf-dag for segment *s45e* (b). Gate *4* is duplicated so that S is free of fanout while Gate *5* and Gate *41* are changed to OR gate and AND gate respectively using De Morgan's law so that the inverters exist only at s along S.

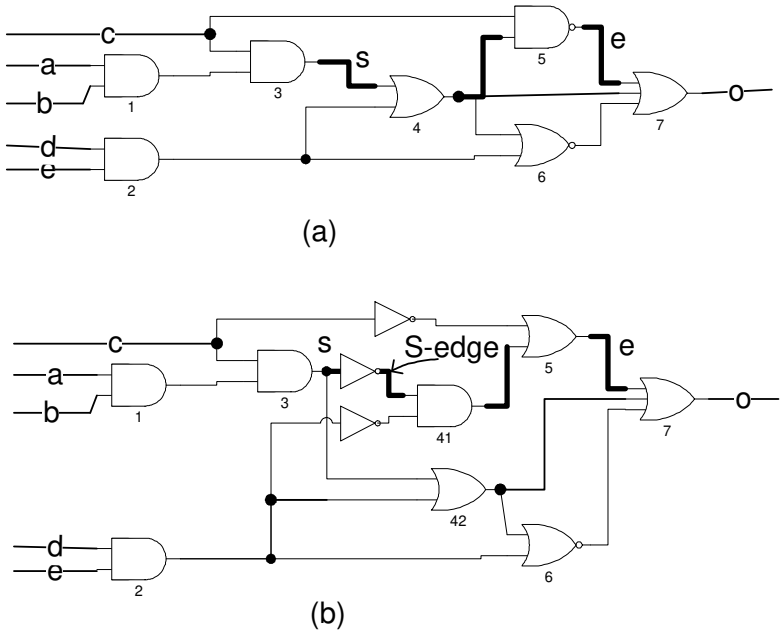

Figure 3: (a)A combinational circuit (b)A segment leaf-dag

Definition 4.5. *A segment transition-smoother STS(Figure 4) is a circuit with inputs V_0 and V_1 and outputs D_0 and D_1. When $V_0 = V_1$, D_0 and D_1 have the same value as V_0 and V_1, respectively. When $V_0 \neq V_1$, D_0 is assigned value 0 while D_1 is assigned value 1. The logic function is summarized as follows.*

V_0	V_1	D_0	D_1
0	*0*	*0*	*0*
0	*1*	*0*	*1*
1	*0*	*0*	*1*
1	*1*	*1*	*1*

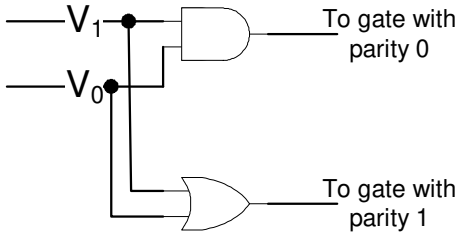

Figure 4: Segment transition-smoother

Definition 4.6. *A segment-leaf-dag C_S^{LD} for segment S can be transformed into a segment-rising-smooth circuit C_S^{RS} (resp. segment-falling-smooth circuit C_S^{FS}) for segment S by the segment-rising-smooth (resp. segment falling-smooth) transformation:*

S1. Analogous to S1 in Definition 3.4 by considering segment S instead of path P and the reverse topological traversal is performed as follows:

Perform a reverse topological traversal of the transitive fanout of the transitive fanout of the primary inputs that are in the transitive fanin of g_1 *on* $S(=\{g_1, g_2, ..., g_m\})$.

S2. Analogous to S2 in Definition 3.4 by considering segment $S(=\{g_1, g_2, ..., g_m\})$ *instead of path* $P(=\{g_1, g_2, ..., g_m\})$.

S3. Let C_{2P} *denote the transformed circuit after the above two steps.* C_{2P} *is called the second pattern partial circuit. Duplicate the transitive fanin of S-edge of* C_{2P} *as* C_{1P}*, which is called the first pattern partial circuit. Each primary input* i_{1P} *in* C_{1P} *has a corresponding primary input* i_{2P} *in* C_{2P}*. Each gate* g_{1P} *in* C_{1P} *has a corresponding* g_{2P} *in* C_{2P}*. Let* s_{2P} *denote the starting point of* S_{2P}*. Insert a segment transition-smoother STS to a primary input* i_{2P} *if* i_{2P} *has an immediate gate with parity 0 or 1 by connecting the inputs* i_{1P} *of* C_{1P} *and* i_{2P} *of* C_{2P} *to the inputs* V_0 *and* V_1 *of STS, respectively and connecting* D_0 *and* D_1 *of STS to the immediate gates with parity 0 and 1, respectively. Note that when the segment S is also a path P, no first partial circuit* C_{1P} *is generated and this step is same as S3 in Definition 3.4.*

Let n denote the number of gates of a given combinational circuit and n_s denote the number of gates along S. Let n'_s denote the number of gates along S that are duplicated where $n'_s \leq n_s$. Note that the size of the resulting circuit after the segment-leaf transformation is $n''' = n + n'_s$ where $n'_s \leq n_s \leq n$. Let n_{sts} denote the number gates resulted from the insertion of STS. During the segment-rising-smooth transformation on the segment leaf-dag with size n''', the gates that are potential to be duplicated in step 2 are gates other than those on S and their duplicates, the number of which is at most $n''' - n_s - n'_s$. Therefore, the size of the resulting circuit after step 2 is at most $2n''' - n_s - n'_s$ or $2n + n'_s - n_s$ for $n''' = n + n'_s$. The number of gates duplicated in step 3 is the number of gates composing the transitive fanin of the starting point of S, which is $n_c \leq 2n - 2n_s$. The number of gates n_{sts} is at most $2n - 2n_s$ as each STS is composed by 2 gates. Therefore, the size of the resulting circuit is $n'''' \leq 2n + n'_s - n_s + n_c + n_{sts} = 6n + n'_s - 5n_s$. The size of the resulting circuit is at most $6n - 5$.

Lemma 4.1. *Let* n *denote the size of a given combinational circuit* C*. The time complexity of the segment-leaf transformation on* C *is* $O(n^2)$.

Proof. Segment-leaf transformation is composed of two steps, which are duplication of each gate along segment S at most once and moving all the inverters on S to the starting point s. The pseudocode is similar to the pseudocode of the single-path-leaf transformation in Lemma 3.1 except that segment S from the starting point s to the ending point e is considered instead of path P from the primary input to the primary output. The pseudocode proves the lemma. □

Lemma 4.2. *Let* C *denote a segment-leaf-dag and* $S \uparrow$ *denote a rising SDF in* C*. The time complexity of the segment rising-smooth transformation on* C *is* $O(n^2)$.

Proof. i_{2P} means a primary input of C while i_{1P} means a primary input of the duplicate of C. $STS(i, j)$ denotes STS with inputs i and j. The following pseudocode proves the lemma.

```
Segment rising-smooth transformation (C, S)
...
 Pseudocodes corresponding to S1 and S2 in Definition 4.6 are
 analogous to those corresponding to S1 and S2 in Definition 3.4 and
 thus are omitted here.
...
```

```
Duplicate the circuit C //2n times
FOR each primary input i //n+1 times
  FOR each G connected to i //2n*n times
    IF the parity of G is 1 THEN
      replace the connection i to G by connection D_1 of STS(i_2P, i_1P) to G
    ELSE IF the parity of G is 0 THEN
      replace the connection i to G by
      connection D_0 of STS(i_2P, i_1P) to G
    END IF
  END FOR
END FOR
```

□

In the following subsection, we will show that the test generation problem for combinational circuits with SDFs is reducible to the test generation problem for its transformed circuits with double SAFs. Therefore, we discuss the time complexity of the double SAF test generation beforehand.

Lemma 4.3. *The test generation complexity for combinational circuits with double SAFs is equivalent to the test generation complexity for combinational circuits with single SAFs, which is τ-equivalent.*

Proof. A circuit with a multiple fault can be represented by a model containing an SAF by adding m extra gates, where m is the multiplicity of the faults. In the case of test generation for combinational circuits with double SAFs, extra two gates are added to the original circuit. Therefore, the test generation for double SAFs has same complexity as that for single SAFs. □

4.1 Test Generation Complexity for Segment Delay Faults

This subsection discusses the test generation complexity for combinational circuits with segment delay faults.

Lemma 4.4. *Let $u + v$ denote the concatenation of vectors u and v, where u consists of a vector at the second pattern primary inputs I_{2P} and v consists of a vector at the first pattern primary inputs I_{1P} of C_S^{RS}. $< u_1, u_2 >=< v_1 + v_1, v_2 + v_1 >$ is a robust test for the $S \uparrow$ in the segment rising-smooth circuit C_S^{RS} for S, if and only if $< v_1, v_2 >$ is a robust test for the $S \uparrow$ in the segment leaf-dag C_S^{LD} for S.*

Proof. **If part:** $< v_1, v_2 >$ is a robust test for the $S \uparrow$ in C_S^{LD} for S. By the definition of robust test, the side-inputs of the OR gates along S in C_S^{LD} are at a steady non-controlling (0) value with no transitions on the application of v_2 after v_1. Let P_S be a set consisting of all the side-paths to OR gates along S. This means the transitions at each I-edge of $Q \in P_S$ do not propagate under the application of $< v_1, v_2 >$. Let u_x^y denote a vector bit of vector u_y at the input x. With the segment transition-smoother in C_S^{RS}, a constant is assigned to the fanout branch of a second pattern primary input i_{2P} according to the parity of the gate connected to the fanout branch if $u_{i_{2P}}^k \neq u_{i_{1P}}^k$ under vector u_k. Let I_{1P} and I_{2P} denote all first pattern primary inputs and all second pattern primary inputs, respectively. Since $u_{I_{1P}}^2 = u_{I_{2P}}^1 = v_1$, a constant is assigned to the fanout branch of a primary input i_{2P} according to the parity of the gate connected to the fanout branch in C_S^{RS}, which has an STS, when there is a transition at i_{2P} ($u_{i_{2P}}^2 \neq u_{i_{2P}}^1$ which also means $u_{i_{2P}}^2 \neq u_{i_{1P}}^2$) under $< u_1, u_2 >$. Since the second pattern partial circuit C_{2P} of C_S^{RS} is functionally equivalent

to C_S^{LD}, the second pattern primary inputs I_{2P} of C_S^{RS} that are assigned with constants under $< u_1, u_2 >$ are corresponding to the primary inputs of C_S^{LD} that have transitions under $< v_1, v_2 >$. Since all the paths from the primary inputs with constants are the paths in P_S in C_S^{RS} and the transitions on the corresponding primary inputs in C_S^{LD} do not propagate to the side-inputs of the OR gates on S, the values of the gates in the transitive fanout of the side-inputs to the OR gates on S_{2P} in C_S^{RS} are same with those on S in C_S^{LS}. Under $u_1(= v_1 + v_1)$, no constants are assigned in C_S^{RS} since $u^1_{I_{2P}} = u^1_{I_{1P}}$ and thus $S \uparrow$ is initialized. Therefore, $< u_1, u_2 >=< v_1 + v_1, v_2 + v_1 >$ is a robust test for the $S \uparrow$ in the segment-rising-smooth circuit C_S^{RS} for S.
Only if part: Since $< u_1, u_2 >=< v_1+v_1, v_2+v_1 >$ is a robust test for S in C_S^{RS}, each side-input to OR gates along S is at a steady non-controlling (0) value. This implies that the constants (assigned according to the parities) asserted on the primary inputs due to $u^1_{i_{2P}} \neq u^2_{i_{2P}}$ do not propagate to the side-inputs of OR gates along S. Since $u^1_{I_{2P}} = v_1$ and $u^2_{I_{2P}} = v_2$ and the second pattern primary inputs I_{2P} in C_S^{RS} that are assigned with constants are corresponding to the primary inputs in C_S^{LD} that have transitions under $< v_1, v_2 >$, the transition on the primary inputs in C_S^{LD} do not propagate to the side-inputs of OR gates along S under $< v_1, v_2 >$. Also, the values of all the gates without parity in the transitive fanout of the side-inputs to the OR gates on S_{2P} in C_S^{RS} and those on S in C_S^{LD} are same. Therefore, $< v_1, v_2 >$ is a robust test for S in C_S^{LD}. □

Lemma 4.5. *$u_2 = v_2 + v_1$ is a test for the double SAF of SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in C_S^{RS} if and only if $< v_1, v_2 >$ is a robust test for $S \uparrow$ in C_S^{LD}.*

Proof. **If part:** Let $< v_1, v_2 >$ be a robust test for the $S \uparrow$ in C_S^{LD}. Then, from Lemma 4.4, $< u_1, u_2 >=< v_1 + v_1, v_2 + v_1 >$ is a robust test for the $S \uparrow$ in C_S^{RS}. The starting point s and the ending point e of S_{2P} are 1 when $u_2(= v_2 + v_1)$ is applied to C_S^{RS} in a fault-free case. This means SA0 is activated and propagated to e. Based on condition 4 of the definition of SDF, the difference at e is propagated to a primary output under $v_2 + v_1$ in C_S^{RS}. Let P_S denote a set consist of all the side-paths to OR gates along S_{2P}. Since the transitions at the I-edges of the paths in P_S do not propagate to the side inputs of OR gates on S_{2P}, the constants assigned to the corresponding primary inputs of those I-edges do not propagate to the side-inputs of OR gates on S_{2P} and also other part of the circuit. So, $v_2 + v_1$ also propagate the fault effect of SA0 at e to the primary output. The partial vector v_1 of $v_1 + v_1$ of $< u_1, u_2 >$ assigns to the S-edge of S_{2P} a value 0 in order to initialize $P \uparrow$. This implies v_1 of $v_2 + v_1$ assigns to the S-edge of S_{1P} a value 0. This activates and propagate the SA1 to the primary output s_{ed}. Hence, $v_2 + v_1$ is a test for the SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in C_S^{RS}.
Only if part: Let $v_2 + v_1$ be a test for the SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in C_S^{RS}. The partial vector v_1 of $v_2 + v_1$ is a test for SA1, which assigns 0 to the S-edge of S_{1P} under the fault free case while the partial vector v_2 is a test for SA0, which assigns 1 to the S-edge of S_{2P} This implies the partial vector v_1 of $v_1 + v_1$ initializes and launches the $S \uparrow$ under $< u_1, u_2 >$. According to the SAF test condition, all the side-inputs of the gates along S_{2P} are at the non-controlling value and the fault effect of S_{2P} propagate to a primary output under $v_2 + v_1$. In order to propagate the fault effect of SA0 at the S-edge of S_{2P}, the constants asserted by the STSs to the primary inputs do not propagate to the side-inputs of the OR gates along S_{2P}. A constant is only asserted to a primary input j if $u^k_{j_{2P}} \neq u^k_{j_{1P}}$. Since $u^2_{j_{1P}} = u^1_{j_{2P}}$, transitions at the primary inputs launched by $< u_1, u_2 >$ do not propagate to the side inputs of OR gates along S. This satisfies the definition of robustly testable SDF. Therefore, $< v_1 + v_1, v_2 + v_1 >$ is a robust test for $S \uparrow$ in C_S^{RS} and according to Lemma 4.4, $< v_1, v_2 >$ is also a robust test for $S \uparrow$ in C_S^{LD} for S. □

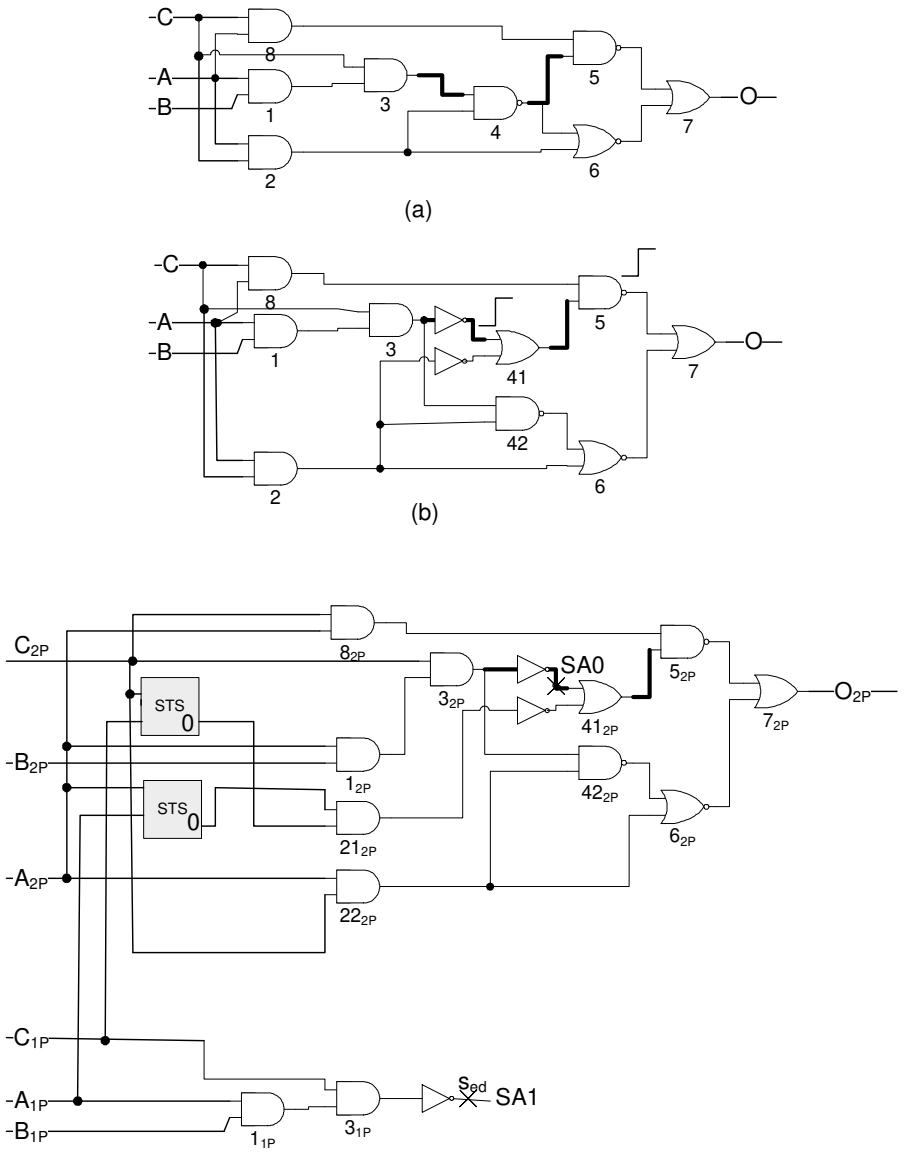

Figure 5: (a)A combinational circuit. (b)A segment leaf-dag. (c)A segment rising-smooth circuit.

Lemma 4.6. *The test generation for combinational circuits with robust SDFs is equivalent to the test generation for segment-rising-smooth circuits with SAFs at S-edges, which is τ-bounded.*

Proof. Lemma 4.4 and Lemma 4.5 show the equivalence of the test generation for combinational circuits with SDFs and its segment rising(falling)-smooth circuits with SAFs at S-edges. Therefore, test generation for combinational circuits using test generation for combinational circuits with SAFs can be performed by the following procedure.

S1. Perform the segment-leaf transformation for segment S on a given combinational circuit C and the resulting circuit C_S^{LD} is called segment-leaf-dag.

S2. Perform the segment-rising-smooth transformation (resp. segment falling-smooth transformation) on C_S^{LD} for segment S and the resulting circuit is C_S^{RS}.

S3. Perform the combinational test generation for SA0 at the S-edge of S and SA1 at the S-edge of S_d in C_S^{RS}. Let $v_1 + v_2$ denote the test.

S4. Transform $v_1 + v_2$ into the robust two-pattern test $< v_1, v_2 >$.

Let n be the size of a given combinational circuit C. Let T_{SL}, T_{SRS}, T_C^{mSA} and T_P denote the time complexity of the segment-leaf transformation, segment-rising-smooth transformation, the test generation for double SAFs and the two-pattern test transformation. Let N_{SL}, N_{SRS}, N_C^{mSA} and N_P denote the problem size of the segment-leaf transformation, segment-rising-smooth transformation, the combinational test generation for double SAFs and the two-pattern test transformation, respectively. According to Lemmas 4.1-4.3 and for $N_{SL} = n$, $n \leq N_{SRS} \leq 2n$, $2n \leq N_C^{mSA} \leq 6n-5$ and $N_P \leq n$. Therefore, the test generation complexity is

$$\begin{aligned} T_C^{rSD}(n) &= T_{SL}(N_{SL}) + T_{SRS}(N_{SRS}) + O(T_C^{mSA}(N_C^{mSA})) + T_P(N_P) \\ &= O(N_{SL}^2) + O(N_{SRS}^2) + O(\tau(N_C^{mSA})) + O(N_P) \\ &\leq O(n^2) + O(4n^2) + O(\tau(6n)) + O(n) \\ &= O(\tau(n)) \end{aligned}$$

□

Figure 5 shows a combinational circuit with a SDF 345 ↑(a), its corresponding segment-leaf-dag for segment 345 (b) and its corresponding segment-rising-smooth circuit for 345. The two-pattern test at the inputs ABC of the original circuit is $< 111, 101 >$.

Theorem 4.1. *The test generation complexity for combinational circuits with robust SDFs is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

Proof. A segment-rising-smooth circuit is also a path rising-smooth circuit when the starting point and the ending point of a segment S are also the primary input and the primary output of the circuit, respectively. Therefore path rising-smooth circuits is a subclass of segment-rising-smooth circuits. To prove this theorem, it is sufficient to show that the test generation for combinational circuits with SAFs can be reduced to the test generation for fanout-inverter-free single-path leaf-dags with robust PDFs, which is a subclass of path rising-smooth circuits. Lemma 3.5 and Lemma 4.6 prove the theorem. □

4.2 Test Generation Complexity for Non-Robust Segment Delay Faults

Definition 4.7. *$C_S^{LD\prime}$ is the transitive fanin of S-edge of C_S^{LD}, which has only one primary output at S-edge.*

Lemma 4.7. *v_2 is a test for the SA0 fault at the S-edge of S in the C_S^{LD} for segment S and v_1 is a test for the SA1 fault on the primary output in the $C_S^{LD\prime}$ if and only if $< v_1, v_2 >$ is a non-robust test for the $S\uparrow$ in C_S^{LD}.*

Proof. **If part:** Let $< v_1, v_2 >$ be a non-robust test for $S\uparrow$ in C_S^{LD}. Consider the presence of SA0 at the S-edge of S in C_S^{LD} under vector v_2. From the definition of non-robust test and SDF, each side-input of S is at a non-controlling value under v_2 and the difference at the ending point e of S under the presence of $S\uparrow$ is propagated to a primary output. Under the fault-free case, the S-edge of S is 1 after the application of v_2. According to test condition, the SA0 fault is activated and the fault effect thus propagates to the same output as the difference at e does in the case of SDF in C_S^{LD}. Hence v_2 is a test for SA0 fault at S-edge of S in C_S^{LD}. Since v_1 assigns 0 to the S-edge of C_S^{LD} in order to initialize the $S\uparrow$, v_1 activates the SA1 fault at the primary output of $C_S^{LD\prime}$, which is corresponding to the S-edge of S in C_S^{LD} and the fault effect propagates to the primary output. **Only if part:** $C_S^{LD\prime}$ is functionally and structurally equivalent to the transitive fanin of the S-edge in C_S^{LD}. Let v_2 be a test for the SA0 on the S-edge of S in C_S^{LD} and v_1 be a test vector for the SA1 at the S-edge of S in $C_S^{LD\prime}$. According to the test condition, 1 is assigned to the primary output in C_S^{LD} and all the side inputs of gates along S in C_S^{LD} are at non-controlling value. The fault effect also propagates to a primary output under v_2. This implies that the difference of the transition caused by $S\uparrow$ taking place at the ending point e of S is observable at the primary output after applying $< v_1, v_2 >$. 0 is assigned to the primary output in $C_S^{LD\prime}$ under v_1. Thus the $S\uparrow$ is initialized. Therefore, $< v_1, v_2 >$ is a non-robust test for $S\uparrow$ in C_S^{LD}. □

Lemma 4.8. *The test generation for combinational circuits with non-robust SDFs is equivalent to the test generation for segment leaf-dags with SAFs at S-edges, which is τ-bounded.*

Proof. Different from test generation for robust SDFs, segment-rising(falling)-smooth transformation is not needed for the test generation for non-robust SDFs. The following procedure explains the test generation for combinational circuits with non-robust SDFs by using the combinational test generation method for SAFs verified by Lemma 4.7 that shows the equivalence of the test generation for combinational circuit with SDFs and that for segment leaf-dag with SAFs:

S1. Perform the segment-leaf transformation for SDFs.

S2. Generate $C_S^{LD\prime}$ from C_S^{LD}.

S3. Generate the second test vector v_2 by the combinational test generation for SA0 (SA1) at the S-edge of S in C_S^{LD}.

S4. Generate the first test vector v_1 by the SAF test generation of SA1 (SA0) at the S-edge of S in $C_S^{LD\prime}$.

S5. Transform v_1 and v_2 into the non-robust two-pattern test $< v_1, v_2 >$.

Let n be the size of a given combinational circuit C. Let T_{SL}, T_C^{mSA} and T_P denote the time complexity of the segment-leaf transformation, test generation for double SAFs and the two-pattern test transformation. Let N_{SL}, N_C^{mSA} and N_P denote the problem size of the segment-leaf transformation, the double SAF combinational test generation and the two-pattern test transformation,

respectively. According to Lemma 4.1 and Lemma 4.3, and also for $N_{SL} = n$, $n \leq N_C^{mSA} \leq 4n$ and $N_P \leq n$. Therefore, the test generation complexity is

$$\begin{aligned} T_C^{nrSD}(n) &= T_{SL}(N_{SL}) + O(T_C^{mSA}(N_C^{mSA})) + T_P(N_P) \\ &= O(N_{SL}^2) + O(\tau(N_C^{mSA})) + O(N_P) \\ &\leq O(n^2) + O(\tau(4n)) + O(n) \\ &= O(\tau(n)) \end{aligned}$$

□

Theorem 4.2. *The test generation complexity for combinational circuits with non-robust SDFs is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

Proof. In order to show that the test generation for combinational circuits with non-robust SDFs and the test generation for combinational circuits with SAFs are equivalent, we need to prove that the test generation for combinational circuits with SAFs is equivalent to the test generation for a subclass of segment leaf-dags with non-robust SDFs besides proving Lemma 4.8. Since segment leaf-dag is a path leaf-dag when the starting point and the ending point of S are also the primary input and the primary output of the circuit, respectively, segment leaf-dags is a superclass of path leaf-dags. Moreover, a robust testable segment delay fault is also a non-robust testable segment delay fault but the converse is not true. Therefore, Lemma 3.5 and Lemma 4.8 are sufficient to prove the theorem. □

5 Test Generation Complexity for Acyclic Sequential Circuits with Stuck-At and Path Delay Faults

Based on the theoretical results in the previous section, we address the reducibility of the test generation for acyclic sequential circuits with PDFs to that for combinational circuits with SAFs. Two clocking schemes are considered here, namely slow-fast-slow clock and rated clock. Slow-fast-slow clocking scheme applies slow clock during justification and propagation while rated clocking scheme requires system clock during all the phases of the test generation. Different from test generation for PDFs, we consider only rated clocking scheme in test generation for SAFs. In the case of the acyclic sequential circuits, which are not internally balanced, slow-fast-slow clock is assumed so that each PDF P in S^A corresponds to only one SDF S in its time expansion model (TEM) $C_E(S^A)$. In the test generation for PDFs, we discuss the processes of transforming an acyclic sequential circuit to its combinational equivalent. From that point, we show the relationships of the test generation for acyclic sequential circuits and that for combinational circuits. Since we have proved that the test generation complexity for combinational circuits with robust and non-robust path delay faults are equivalent, for simplicity we denote the robust and non-robust path delay faults as path delay faults.

5.1 Balanced Sequential Circuits

[2]Let a directed graph $G = (V, A, H)$ represents a sequential circuit. V represents a set of clouds where each cloud is a maximal region of connected combinational logic such that its inputs are either primary inputs or outputs of registers and its outputs are either primary outputs of inputs to registers. A represents a set of connections between two clouds through a register. Arcs in $H \subset A$ represent $HOLD$ registers. A sequential circuit is said to be a balanced sequential circuit if

C1. G is acyclic;

C2. $\forall v_i, v_j \in V$, all directed paths (if any) from v_i to v_j are of equal length;

C3. $\forall h \in H$, if h is removed from G, the resulting graph is disconnected.

5.1.1 Test Generation Complexity for Stuck-At Faults

Previous work[2] showed that a balanced sequential circuit can be transformed polynomially into its combinational equivalent by replacing all flip-flops by wires, proving the equivalence of the test generation for balanced sequential circuits with stuck-at faults and its combinational equivalents with stuck-at faults.

Theorem 5.1. *The test generation complexity for balanced sequential circuits with SAFs is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

5.1.2 Test Generation Complexity for Path Delay Faults

Definition 5.1. [8] *Let G be a circuit graph of a balanced sequential circuit $\mathcal{S}^{\mathcal{B}}$. The following discussion considers only one output cone circuit $\mathcal{S}_{\mathcal{C}}^{\mathcal{B}}$ of $\mathcal{S}^{\mathcal{B}}$, which is a strongly balanced structure. Let $t(q_i)$ be an integer value which can be assigned to a vertex q_i such that it satisfies the condition of the strongly balanced structure.*

$$t(v_i) = t(v_j) + w(a) \ \forall a(v_i, v_j). \tag{1}$$

Let t_{max} and t_{min} be the maximum value and the minimum value among the integer values assigned to the vertices of G, respectively. Let I_j $(j = 1, 2, ..., p)$ be a vertex, which corresponds to an input of the output cone circuit $\mathcal{S}_{\mathcal{C}}^{\mathcal{B}}$. A vector $T_I = (\alpha_1, \alpha_2, ..., \alpha_p)$ such that $\alpha_j = t_{max} - t(I_j) + 1$ is said to be an input timing vector of the output cone circuit $\mathcal{S}_{\mathcal{C}}^{\mathcal{B}}$. Let L be $t_{max} - t_{min} + 2$. Let $< v_1, v_2 >$ be a p-bit vector pair where a vector v_l is $(v_1^l, v_2^l, ..., v_j^l, ..., v_p^l)$. A vector sequence $[x_{ij}]$ of length L such that

$$x_{ij} = \begin{cases} v_j^1 & \text{if } i = \alpha_j \\ v_j^2 & \text{if } i = \alpha_j + 1 \\ \text{don't care} & \text{otherwise} \end{cases} \tag{2}$$

is said to be an extended vector sequence of $< v_1, v_2 >$ with respect to T_I. A transformation M which transforms from $< v_1, v_2 >$ into the extended vector sequence with respect to T_I is referred to as sequence transformation with respect to T_I.

Lemma 5.1. *Let $< v_1, v_2 >$ denote a two-pattern test of a given balanced sequential circuit with size n. The time complexity of the sequence transformation on $< v_1, v_2 >$ is $O(n)$.*

Proof. Let G be a circuit graph of a balanced sequential circuit with sequential depth $L - 2$ and let $< v_1, v_2 >$ be a pair of input vectors of p bits, where $L \leq n$ and $p \leq n$. Let N_V denote the number of vertices in the circuit graph where $N_V \leq n$.

```
Sequence transformation (G, v1, v2)                          times
                                                            (at most)
  FOR each vertex u                                          N_V+1
    Assign to u an integer t so that equation 1 is satisfied
  END FOR
  Compute input timing vector T_I                              p
  FOR j from 1 to p                                            n
    Compute α_j
    Compute i
    Compute x_ij
  END FOR
```

The pseudocode proves the lemma. □

Theorem 5.2. [8] *The test generation problem for PDF list F^B of a balanced sequential circuit $\mathcal{S}^{\mathcal{B}}$ can be reduced to the test generation problem for SDF list F^{CB} of its combinational equivalent $C(\mathcal{S}^{\mathcal{B}})$.*

According to Theorem 5.2, the test generation for balanced sequential circuits with PDFs is equivalent to the test generation for its combinational equivalents with SDFs. In the previous section, we showed that the test generation for combinational circuits with SDFs can be reduced to the test generation for its segment-leaf-dags with non-robust PDFs or its segment-rising(falling)-smooth circuits with robust PDFs. The following procedure generates a PDF test for a balanced sequential circuit using combinational test generation for SAFs.

S1. Transform the given circuit into its combinational equivalent $C(\mathcal{S}^{\mathcal{B}})$.

S2. Follow the procedures of test generation for combinational circuits with robust and non-robust SDFs. Let $< v_1, v_2 >$ denote the resulting two-pattern test.

S3. Transform $< v_1, v_2 >$ into the two-pattern test sequence using the sequence transformation [8].

Based on Theorem 5.2, the theorems and lemmas of the test generation for combinational circuits with SDFs, we conclude the following theorem.

Theorem 5.3. *The test generation complexity for balanced sequential circuits with PDFs under rated clock and slow-fast-slow clock is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

5.2 Internally Balanced Sequential Circuits

According to [1], a circuit resulting from operation 1 of the extended combinational transformation (C^*-transformation) on an acyclic sequential circuit is a balanced sequential circuit, then the circuit is regarded as an internally balanced sequential circuit. C^*-transformation consists of the following two operations.

S1. For a primary input with fanout branches, the set of fanout branches of that primary input is denoted by X. Let us obtain the smallest partition of X which satisfies the following statement: If branches x_i and x_j belong to different blocks $X(i)$, $X(j)$ of partition $\prod(x_i \subset X(i), x_j \subset X(j), X(i) \neq X(j))$, then x_i and x_j are separable. Each partitioned block is provided with a new primary input separated from the original primary input;

S2. All flip-flops are replaced by wires.

5.2.1 Test Generation Complexity for Stuck-At Faults

[1] has proved that if a fault f in an internally balanced sequential circuit, can be tested then the corresponding fault f_C in $C^*(S)$ can be tested. And, there is no logic duplication in C^*-transformation. $C^*(S)$ can be done in time $O(n^2)$.

Theorem 5.4. *The test generation complexity for internally balanced sequential circuits with SAFs is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

5.2.2 Test Generation Complexity for Path Delay Faults

In this section, we discuss the test generation complexity for internally balanced sequential circuits. We discuss the sequence transformation [9] in Definition 5.2, the lemma and definitions on pattern dependency in Lemma 5.2-5.4, and Definitions 5.3-5.5, respectively. These lemmas and definitions also apply in the discussion in Section 5.3.2.

Definition 5.2. [9] *Let $\mathcal{S}^{\mathcal{A}}$ be an acyclic sequential circuit, and let $G = (V, A, w)$ be the topology graph of $\mathcal{S}^{\mathcal{A}}$. Let $E = (V_E, A_E, t, l)$ be a TEG of G, and let $C_E(\mathcal{S}^{\mathcal{A}})$ be the TEM of $\mathcal{S}^{\mathcal{A}}$ based on E. Let t_{min} be the minimum value of labels assigned to vertices in E, and let d be the sequential depth of $\mathcal{S}^{\mathcal{A}}$. Let $< v_u^1, v_u^2 >$ be a two-pattern vector at a primary input $u \in V_E$ in $C_E(\mathcal{S}^{\mathcal{A}})$. A procedure transforming $< v_u^1, v_u^2 >$ into the input pattern to the primary input $l(u) \in V$ of $\mathcal{S}^{\mathcal{A}}$ at time k (=0, 1, ..., $d+1$) denoted as $I_{l(u)}(k)$ is said to be the sequence transformation γ. That is, for each u,*

$$I_{l(u)}(k) = \begin{cases} v_u^1 & \text{if } k = t(u) - t_{min} \\ v_u^2 & \text{if } k = t(u) - t_{min} + 1 \\ \textit{don't care} & \textit{otherwise} \end{cases} \tag{3}$$

Such an input sequence with the length $d+2$ is regarded as a two-pattern input sequence.

Lemma 5.2. *Let x and y denote two different primary inputs of $C_E((\mathcal{S})^{\mathcal{A}})$. To avoid conflicts during sequence transformation γ, $v_x^2 = v_y^1$ if $l(x) = l(y) = z$ and $t(y) - t(x) = 1$.*

Proof.

$$I_{l(x)}(k) = \begin{cases} v_x^1 & \text{if } k = t(x) - t_{min} \\ v_x^2 & \text{if } k = t(x) - t_{min} + 1 \\ \text{don't care} & \textit{otherwise} \end{cases} \tag{4}$$

$$I_{l(y)}(k) = \begin{cases} v_y^1 & \text{if } k = t(y) - t_{min} \\ v_y^2 & \text{if } k = t(y) - t_{min} + 1 \\ \text{don't care} & \textit{otherwise} \end{cases} \tag{5}$$

Let $l(x) = l(y) = z$ and $t(y) - t(x) = 1$. Then,

$$I_{l(y)}(k) = I_z(k) = v_y^1 \text{ if } k = t(y) - t_{min} = t(x) - t_{min} + 1 \tag{6}$$

Since $l_{l(x)}(k) = l_z(k) = v_x^2$ if $k = t(x) - t_{min} + 1$, $v_x^2 = v_y^1$. □

Definition 5.3. *Let x and y denote two different primary inputs of $C_E((\mathcal{S})^{\mathcal{A}})$. x and y are called pattern-dependency input pair (x,y) if $l(x) = l(y) = z$ and $t(y) - t(x) = 1$.*

Definition 5.4. *Given a segment leaf dag $C_S^{LD}((\mathcal{S})^{\mathcal{A}})$ of a TEM $C_E(\mathcal{S}^{\mathcal{A}})$ of $\mathcal{S}^{\mathcal{A}}$, the circuit can be transformed into a pattern-dependency circuit $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ by the pattern-dependency transformation.*

S1. In the case of non-robust test generation, duplicate the transitive fanin of S-edge of C_S^{LD} where the segment leaf dag C_S^{LD} becomes the second pattern partial circuit C_{2P} while the duplicate becomes the first pattern partial circuit C_{1P}. In the case of robust test generation, perform the segment-rising-smooth (resp. segment-falling-smooth) transformation.

S2. For each pattern-dependency input pair (x, y) of $C_E(\mathcal{S}^{\mathcal{A}})$, connect the corresponding x_{2P} and y_{1P} to form a new primary input called unified input w. The resulting circuit is called pattern-dependency circuit $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$.

The idea of pattern-dependency was introduced in [10].

Definition 5.5. *Given a pattern-dependency circuit $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$. Let C_{1P} and C_{2P} denote the first pattern partial circuit and the second pattern partial circuit of $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$, respectively. Let $v_1^1, v_2^1, ..., v_m^1$ of an m-bit vector v_1 denote a vector bit at each primary input of C_{1P} of $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ or the stem of the primary input fanout branches fed to C_{1P} of $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ if the input is a unified input, respectively where m is the number of vector bits. Let $v_1^2, v_2^2, ..., v_m^2$ of an m-bit vector v_2 denote a vector bit at each primary input of C_{2P} of $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ or the stem of the primary input fanout branches fed to C_{2P} of $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ if the input is a unified input, respectively where m is the number of vector bits. $d(v_1, v_2)$ denote the input vector of the pattern-dependency circuit $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$.*

In the following Lemma 5.3 and 5.4, only rising SDF is discussed. The lemmas and proofs for falling SDF can be derived by considering SA1 at the S-edge of S_{2P} and SA0 at the S-edge of S_{1P} in $C_S^{PD}(S^A)$.

Lemma 5.3. *$< v_1, v_2 >$ is a robust(resp. non-robust) test for the $S \uparrow$ in $C_S^{LD}(\mathcal{S}^{\mathcal{A}})$ if and only if $d(v_1, v_2)$ is a test for SA0 at the S-edge of the corresponding segment S_{2P} and SA1 at the S-edge of the corresponding S_{1P} in $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ with (resp. without) STS.*

Proof. **If part:** Let $d(v_1, v_2)$ be a test for SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$. S-edge of S_{2P} is assigned a value 1 while S-edge of S_{1P} is assigned a value 0 under $d(v_1, v_2)$. Based on the definition of the pattern dependency transformation, this implies a rising transition is launched at the S-edge of S under $< v_1, v_2 >$ in C_S^{LD}. According to the test condition, all the side inputs along S_{2P} are at the non-controlling values under the partial vector v_2. This satisfies condition 1 of the robust test and definition of the non-robust test that the transition launched at the S-edge of S propagates to the ending point of S under $< v_1, v_2 >$. With segment-transition-smoothers (STSs) in the case of the robust test, the constants assigned to the primary inputs of $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ do not propagate to the side-inputs of the OR gates along S_{2P} under $d(v_1, v_2)$. This means no transitions are at the side inputs of the OR gates along S in $C_S^{LD}(\mathcal{S}^{\mathcal{A}})$ under $< v_1, v_2 >$. Condition 2 of the robust test is satisfied. The fault effect of SA0 at the S-edge of S_{2P} is propagated to a primary output under the partial vector v_2. Thus the difference caused by $S \uparrow$ at the ending point of S propagates to the primary output under $< v_1, v_2 >$. Therefore, $< v_1, v_2 >$ is a robust(resp. non-robust) test for the $S \uparrow$ in $C_S^{LD}(\mathcal{S}^{\mathcal{A}})$.
Only if part: Let $< v_1, v_2 >$ be a robust(resp. non-robust) test for the $S \uparrow$. The S-edge of S is assigned a value 0 under vector v_1 and 1 under vector v_2. Thus the SA0 at the S-edge of S_{2P} and the SA1 at the S-edge of S_{1P} in $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ are activated under the vector $d(v_1, v_2)$. The fault effect of SA1 at the S-edge of S_{1P} propagates to the primary output s_{ed}. The fault effect of SA0 at the S-edge of S_{2P} propagates to a primary output since all the side-inputs along S_{2P} are at the non-controlling values and the difference at the ending point of S_{2P} propagate to the primary output under $d(v_1, v_2)$. □

Lemma 5.4. *Let P be a path in a given acyclic sequential circuit $\mathcal{S}^{\mathcal{A}}$ and let S_{2P} and S_{1P} be the corresponding segments in its pattern-dependency circuit $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$. Let (v_1, v_2) be a pattern-dependency input pair. Let $\gamma_L(v_1, v_2)$ denote a two-pattern sequence of length L transformed from the two-pattern vector $< v_1, v_2 >$ by the sequence transformation γ. $\gamma_L(v_1, v_2)$ is a robust(resp. non-robust) two-pattern sequence for the $P \uparrow$ in $\mathcal{S}^{\mathcal{A}}$ with sequential depth $L-2$ if and only if $d(v_1, v_2)$ is a test for SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ with (resp. without) STS.*

Proof. **If part:** Let $d(v_1, v_2)$ be a test for SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$. From Lemma 5.4, $< v_1, v_2 >$ is a robust(resp. non-robust) test for the corresponding $S \uparrow$ in $C_S^{LD}(\mathcal{S}^{\mathcal{A}})$ and thus in $C_E(\mathcal{S}^{\mathcal{A}})$. Let c be the combinational block in $C_S^{LD}(\mathcal{S}^{\mathcal{A}})$ that contains $S \uparrow$ is and let $< v_c^1, v_c^2 >$ be the two-pattern vector at the inputs I_c of c under $< v_1, v_2 >$. $S \uparrow$ is launched and propagates to an output of c under $< v_c^1, v_c^2 >$. Therefore, the fault effect of $S \uparrow$ is at the ending point of S. c in $C_E(\mathcal{S}^{\mathcal{A}})$ and $l(c)$ in $\mathcal{S}^{\mathcal{A}}$ are logically same. According to Lemma 5.3, there is no pattern conflict in transforming $< v_1, v_2 >$ into $\gamma_L(v_1, v_2)$ since v_1 and v_2 are generated from the pattern-dependency circuit. According to the sequence transformation γ, $I_{l(c)} = v_c^1$ at time $t(c) - t_{min}$, $I_{l(c)} = v_c^2$ at time $t(c) - t_{min} + 1$. Therefore, the $P \uparrow$ in $\mathcal{S}^{\mathcal{A}}$ which corresponds to the $S \uparrow$ in $C_E(\mathcal{S}^{\mathcal{A}})$ is launched and propagates to the output of $l(c)$. The fault effect of $S \uparrow$ at the output of c propagates to a primary output o under $< v_1, v_2 >$. According to Definition 5.2, the fault effect of the $P \uparrow$ propagates to the primary output $l(o)$ at time $t(o) - t_{min} + 1$ under the two-pattern input sequence $\gamma_L(v_1, v_2)$.
Only if part: Let $\gamma_L(v_1, v_2)$ be the two-pattern test sequence for the $P \uparrow$. According to Definition 5.2, $\gamma_L(v_1, v_2)$ can be inverse transformed to a two-pattern vector $< v_1, v_2 >$ that activates the corresponding $S \uparrow$ in $C_E(\mathcal{S}^{\mathcal{A}})$ and propagates the fault effect to a primary output by the inverse transformation γ^{-1}. Therefore, $d(v_1, v_2)$ is a test for SA0 at the S-edge of S_{2P} and SA1 at the S-edge of S_{1P} in $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$. □

Theorem 5.5. *The test generation complexity for internally balanced sequential circuits with PDFs under rated clock and slow-fast-slow clock is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

Proof. The following procedure of test generation for acyclic sequential circuits of sequential depth $d = L - 2$, with PDFs can be used as shown by Lemmas 5.3 and 5.4.

S1. Generate a TEM of $\mathcal{S}^{\mathcal{A}}$;

S2. For each $P \uparrow$ (resp. $P \downarrow$),

- S2.1. Perform the segment-leaf transformation on $C_E(\mathcal{S}^{\mathcal{A}})$. The resulting circuit $C_S^{LD}(\mathcal{S}^{\mathcal{A}})$ is called segment-leaf-dag.
- S2.2. Perform the pattern-dependency circuit transformation. The resulting circuit $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$ is called pattern-dependency circuit.
- S2.3. Perform the combinational test generation for SA0 (resp. SA1) at the S-edge of S_{2P} and SA1 (resp. SA0) at the S-edge of S_{1P} in the pattern-dependency circuit $C_S^{PD}(\mathcal{S}^{\mathcal{A}})$. Let $d(v_2, v_1)$ denote the test obtained respectively.
- S2.4. Split $d(v_1, v_2)$ into v_1 and v_2 according to the definition of $d(v_1, v_2)$. Transform $< v_1, v_2 >$ into the two-pattern sequence $\gamma_L(v_1, v_2)$ based on Definition 5.2.

Let T_{SL}, T_{PD}, T_C^{mSA} and T_P denote the time complexity of the segment-leaf transformation, the pattern-dependency circuit transformation, the test generation for double SAFs and the two-pattern sequence transformation, respectively. Let N_{SL}, N_{PD}, N_C^{mSA} and N_P denote the problem size of the segment-leaf transformation, the pattern-dependency circuit transformation, the double SAF test generation and the two-pattern sequence transformation, respectively. According to Lemma 5.1 and Lemma 4.1-4.3 and for $N_{SL} = n$, $n \leq N_{PD} \leq 2n$, $2n \leq N_C^{mSA} \leq 6n-5$, $N_P \leq n$. Therefore, the test generation complexity is

$$\begin{aligned} T_{IB}^{PD}(n) &= T_{SL}(N_{SL}) + T_{PD}(N_{PD}) + O(T_C^{mSA}(N_C^{mSA})) + T_P(N_P) \\ &= O(N_{SL}^2) + O(N_{PD}^2) + O(\tau(N_C^{mSA})) + O(N_P^2) \\ &\leq O(n^2) + O(4n^2) + O(\tau(6n)) + O(n^2) \\ &= O(\tau(n)) \end{aligned}$$

Therefore, the test generation for internally balanced sequential circuits with PDFs is equivalent to the test generation for pattern dependency circuits with SAFs at S-edges, which is τ-bounded. To show that the test generation for internally balanced sequential circuits with PDFs is τ-equivalent, we have to prove that the test generation for combinational circuits with SAFs is equivalent to that for a subclass of internally balanced sequential circuits with SAFs. Since test generation for balanced sequential circuits with PDFs is τ-equivalent and test generation for internally balanced sequential circuits with PDFs is shown τ-bounded in the above-mentioned lemma, the test generation for internally balanced sequential circuits with PDFs is equivalent to the test generation for combinational circuits with SAFs, which is τ-equivalent. □

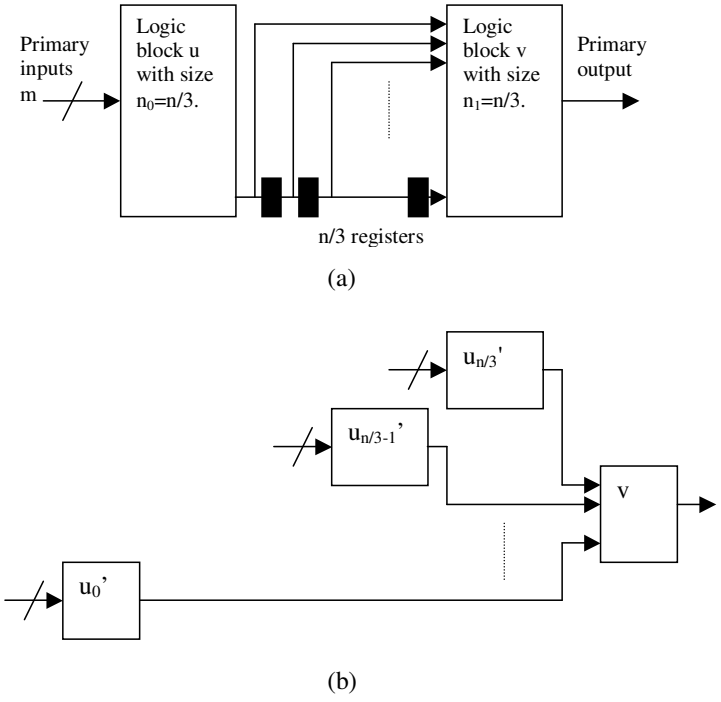

Figure 6: (a)Acyclic sequential circuit S^{A1}. (b)Its time expansion model

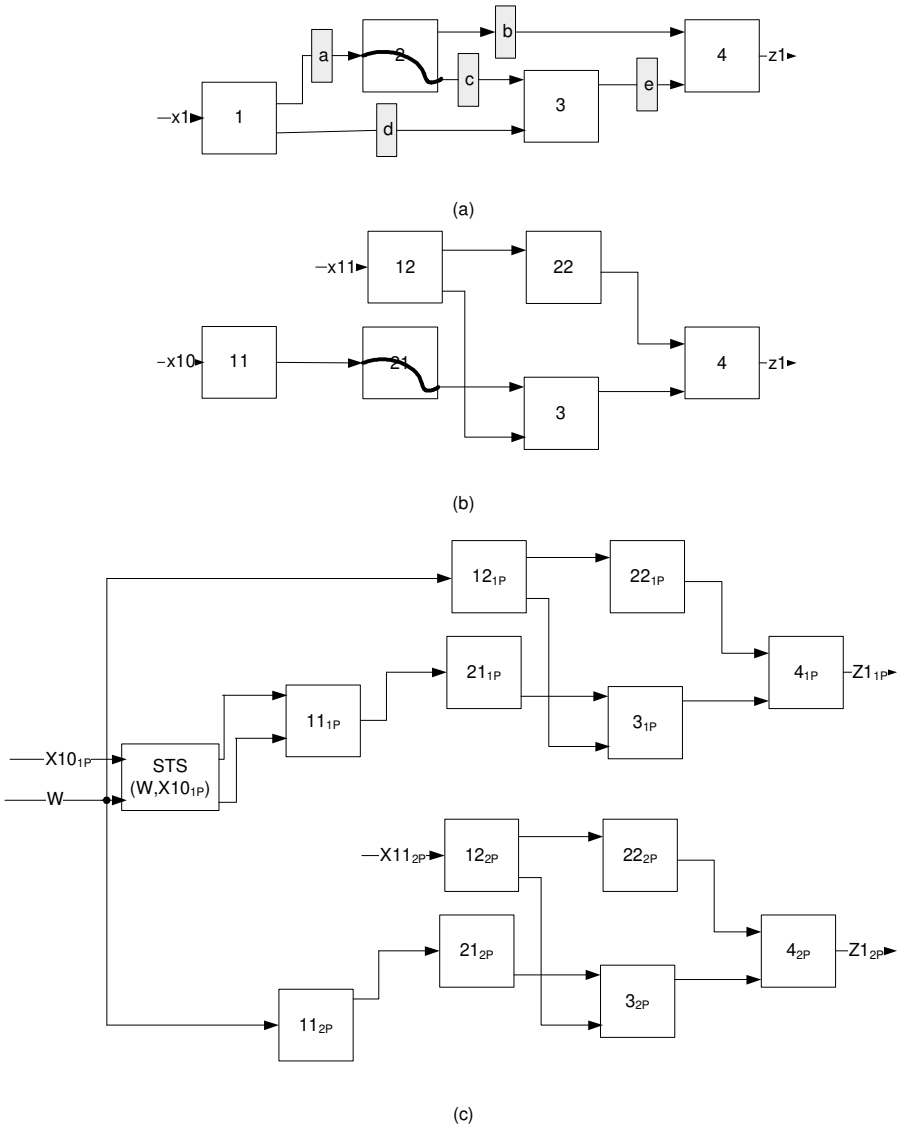

Figure 7: (a) An acyclic sequential circuit. (b) Its time expansion model. (c) Its pattern-dependency circuit.

5.3 Acyclic Sequential Circuits

In this section, we discuss about the test generation complexity for acyclic sequential circuits with SAFs and PDFs.

Definition 5.6. *S^{A1} is an acyclic sequential circuit that satisfies the following conditions (Figure 6(a)).*

C1. It has the following topology graph $G = (V, A, r)$.

C1.1. $V = \{u, v\}$ where $u \in pre(v)$ and $A = \{a_i | 0 \leq i \leq \frac{n}{3}\}$;

C1.2. $r_i(u, v) = i$ for $0 \leq i \leq \frac{n}{3}$ where $r_i(u, v)$ represents a label on arc a_j and $\frac{n}{3}$ is the sequential depth of S^{A1}.

C2. Let n_0 and n_1 be the size of the logic block represented by vertices u and v, respectively where $n_0 = n_1 = \frac{n}{3}$.

Its time expansion model is shown in Figure 6(b).

5.3.1 Test Generation Complexity for Stuck-At Faults

Theorem 5.6. *The test generation complexity for acyclic sequential circuits with SAFs is τ^2-bounded.*

Proof. The number of time frames in which logic duplication might take place is at most d, where d is the sequential depth. The time complexity for logic duplication is $O(n(d+1))$. Thus, the test generation complexity for acyclic sequential circuits with SAFs is

$$\begin{aligned} T_A(n) &= O(n(d+1)) + \tau(n(d+1)) \\ &= O(\tau^2(n)) \text{ for } d \leq n \end{aligned}$$

□

We found out the acyclic sequential circuits S^{A1} where its test generation complexity for stuck-at faults under TEM is not τ-equivalent.

Theorem 5.7. *The test generation complexity for acyclic sequential circuits with SAFs under TEM is not τ-equivalent.*

Proof. Vertex u in the topology graph of S^{A1} is mapped to $(\frac{n}{3}+1)$ different vertices in TEM. Note that no logic portion of $u_i{}'$ is removed. Thus the size of the combinational equivalent of the acyclic sequential circuit represented by the TEM is

$$\begin{aligned} N &= \frac{n}{3}(\frac{n}{3}+1) + \frac{n}{3} \\ &= \frac{n^2}{9} + \frac{2n}{3} \end{aligned}$$

Therefore, the test generation complexity for S^{A1} is

$$\begin{aligned} T_{A1} = \tau(N) &= \tau(\frac{n^2}{9} + \frac{2n}{3}) \\ &= \Theta(\tau(n^2)) \end{aligned}$$

The test generation complexity for acyclic sequential circuit S^{A1} with SAFs under TEM is not τ-equivalent. □

However, there might be other test generation models for acyclic sequential circuits besides TEM. "Is T_A τ-equivalent?" remains an open problem. No one has proved the answer is "Yes" but it seems to be "No" based on the above-mentioned theorem. Therefore, we have the following conjecture.

Conjecture 5.1. *The test generation complexity for acyclic sequential circuits with SAFs is not τ-equivalent.*

5.3.2 Test Generation Complexity for Path Delay Faults

The test generation complexity for acyclic sequential circuits with path delay faults is discussed under slow-fast-slow clock. The case of rated clock is important in at-speed testing. Thus, we identify and state the open problems related to the case of rated clock.

Theorem 5.8. *The test generation complexity for acyclic sequential circuits with PDFs under slow-fast-slow clock is τ^2-bounded.*

Proof. Let T_{SL}, T_{PD}, T_C^{mSA} and T_P denote the time complexity of the segment-leaf transformation, the pattern-dependency circuit transformation, the test generation for double SAFs and the two-pattern sequence transformation, respectively. Let N_{SL}, N_{PD}, N_C^{mSA} and N_P denote the problem size of the segment-leaf transformation, the pattern-dependency circuit transformation, the test generation for double SAFs and the two-pattern sequence transformation, respectively. Let $\mathcal{S}^{\mathcal{A}}$ denote a given acyclic sequential circuit. The size of its TEM $C_E(\mathcal{S}^{\mathcal{A}})$ is $(d+1)n$ where d is the sequential depth. For $n \leq N_{SL} \leq (d+1)n$, $n \leq N_{PD} \leq 2((d+1)n)$, $2n \leq N_C^{mSA} \leq 6((d+1)n) - 5$, $N_P \leq n$. Therefore, the test generation complexity is

$$\begin{aligned} T_A^{PD}(n) &= T_{SL}(N_{SL}) + T_{PD}(N_{PD}) + T_C^{mSA}(N_C^{mSA}) + T_P(N_P) \\ &= O(N_{SL}^2) + O(N_{PD}^2) + O(\tau(N_C^{mSA})) + O(N_P^2) \\ &= O(d^2n^2) + O(4d^2n^2) + O(\tau(6dn)) + O(n^2) \\ &= O(\tau^2(n)) \text{ for } d = O(n) \end{aligned}$$

□

Besides the test generation for PDFs under slow-fast-slow clock, there are analogous issue for the case under rated clock testing.

Open Problem 5.1. *Is the test generation complexity for acyclic sequential circuits with PDFs under rated clock τ^2-bounded?*

Theorem 5.9. *The test generation complexity for acyclic sequential circuits with PDFs under TEM at slow-fast-slow clock is not τ-equivalent.*

Proof. By using the example of S^{A1}, we show that the test generation complexity for acyclic sequential circuits with path delay faults under TEM at slow-fast-slow clock is not τ-equivalent. Vertex u in the topology graph for S^{A1} is mapped to $(\frac{n}{3}+1)$ different vertices in TEM. Note that no logic portion of $u_i{}'$ is removed. From its TEM, the corresponding pattern-dependency circuit is obtained. The size of the pattern-dependency circuit is at most the total of the size of the first pattern partial circuit and the size of the second pattern partial circuit.

$$N \leq (\frac{n}{3}(\frac{n}{3}+1) + \frac{n}{3}) + (\frac{n}{3})$$

$$\frac{n^2}{9} + \frac{2n}{3} \leq N \leq \frac{n^2}{9} + n$$

The test generation for S^{A1} with path delay faults under TEM at slow-fast-slow clock is equivalent to the test generation for its equivalent pattern-dependency circuits with stuck-at faults at S-edges. Therefore, the test generation complexity for S^{A1} is

$$\begin{aligned} T_{A1} = O(\tau(N)) &= O(\tau(\frac{n^2}{9} + n)) \\ &= O(\tau(n^2)) \end{aligned}$$

The test generation problem for a subclass of combinational circuits with SAFs at primary input is a subproblem of the test generation problem for a subclass of combinational circuits with SAFs at S-edges since an S-edge becomes I-edge when the segment is also a path and I-edge can be a primary input. Therefore, from Lemma 3.6,

$$\begin{aligned} T_{A1} = \Theta(\tau(N)) &= \Theta(\tau(\frac{n^2}{9} + n)) \\ &= \Theta(\tau(n^2)) \end{aligned}$$

□

There might be also other test generation models for acyclic sequential circuits with PDFs besides TEM. Consequently, we have the following conjecture.

Conjecture 5.2. *The test generation complexity for acyclic sequential circuits with PDFs under slow-fast-slow clock is not τ-equivalent.*

We also have not yet considered the case under rated clock. Open Problem 5.2 corresponds to Theorem 5.9 while Open Problem 5.3 corresponds to Conjecture 5.2.

Open Problem 5.2. *Is the test generation complexity for acyclic sequential circuits with PDFs under TEM with rated clock τ-equivalent?*

Open Problem 5.3. *Is the test generation complexity for acyclic sequential circuits with PDFs under rated clock τ-equivalent?*

Example Figure 7 shows the transformations of an acyclic sequential circuit to represent its test generation problem for PDFs based on the test generation for SAFs. Note that only one PDF is considered, that is in block 21, under slow-fast-slow clock.

We have shown that the test generation problems for SAFs and PDFs are equivalent for combinational circuits, balanced sequential circuits, and internally balanced sequential circuits. We only showed that they are not equivalent for acyclic sequential circuits under TEM. Therefore, we still have the following open problem.

Open Problem 5.4. *Is the test generation complexity for acyclic sequential circuits with PDFs under rated clock equivalent to the test generation complexity for acyclic sequential circuits with SAFs?*

The solutions of these open problems are useful in ATPG and DFT development.

6 Test Generation Complexity for Cyclic Sequential Circuits with Stuck-At and Path Delay Faults

In this section, we introduce several easily testable classes of cyclic sequential circuits and discuss their test generation complexity for SAFs and PDFs.

6.1 Easily Testable Classes of Cyclic Sequential Circuits

We consider that a class is easily testable if its test generation complexity is τ^2-bounded. In other words, τ^2-bounded classes and τ-equivalent classes are easily testable. In the previous section, we have shown that acyclic sequential circuits is easily testable. In this section, we introduce several classes of easily testable cyclic sequential circuits.

Generally, the test generation for cyclic sequential circuits with stuck-at faults (resp. path delay faults) involves the following three steps.

S1. Derivation of the stuck-at fault (resp. path delay fault) excitation state. Two time frames are considered for the derivation of the path delay fault excitation state;

S2. State justification; and

S3. State differentiation.

Backtracks may occur between the three steps and within each step. However, there exist classes of sequential circuits where no backtracks occur between these three steps. In such case, it is guaranteed that any excitation state can be justified and any excited fault can be propagated to a primary output. The time complexity for derivation of excitation state is τ-equivalent for SAFs and PDFs. The time complexity for derivation of PDF excitation state will be discussed in details in Section 6.3. Therefore, if the state justification and the state differentiation can be reduced to the problems that are τ^2-bounded or τ-equivalent, the circuits are easily testable.

We define four easily testable classes of sequential circuits based on the number of time frames and the time complexity taken by the state justification and state differentiation, and the state validity.

Definition 6.1. *A sequential circuit S is l-length-bounded testable with respect to a fault set F if the following conditions are satisfied.*

C1. For any state s_i, there exists a state justification sequence of length at most l;

C2. For any pair of states (s_i, s_{if}), there exists a state differentiation sequence of length at most l, where s_i is a fault-free state and s_{if} is a faulty state corresponding to a fault $f \in F$.

Definition 6.2. *A sequential circuit S is l-length-bounded validity-identifiable with respect to a fault set F if the following conditions are satisfied.*

C1. There exists a combinational circuit of size $O(n)$ called validity checker that can identify the validity states, where n is the size of the sequential circuits;

C2. For any valid state s_i, there exists a state justification sequence of length at most l from initial state s_0;

C3. For any pair of states (s_i, s_{if}), there exists a state differentiation sequence of length at most l, where s_i is a fault-free valid state and s_{if} is a faulty state corresponding to a fault $f \in F$.

Definition 6.3. *A sequential circuit S is t-time-bounded testable with respect to a fault set F if the following conditions are satisfied.*

C1. For any state s_i, there exists a state justification sequence which can be obtained in time $O(t)$;

C2. For any pair of states (s_i, s_{if}), there exists a state differentiation sequence which can be obtained in time $O(t)$, where s_i is a fault-free state and s_{if} is a faulty state corresponding to a fault $f \in F$.

Definition 6.4. *A sequential circuit S is t-time-bounded validity-identifiable with respect to a fault set F if the following conditions are satisfied.*

C1. There exists a combinational circuit of size $O(n)$ called validity checker that can identify the validity of states, where n is the size of the sequential circuits;

C2. For any valid state s_i, there exists a state justification sequence from initial state s_0 which can be obtained in time $O(t)$;

C3. For any pair of states (s_i, s_{if}), there exists a state differentiation sequence which can be obtained in time $O(t)$, where s_i is a fault-free valid state and s_{if} is a faulty state corresponding to a fault $f \in F$.

It is obvious from Definition 6.1-6.4 that in both cases of SAFs and PDFs, the test generation complexity for l-length-bounded testable circuits with $l = O(n)$, l-length-bounded validity-identifiable circuits with $l = O(n)$, t-time-bounded testable circuits with $t = \tau^2(n)$ and t-time-bounded validity-identifiable circuits with $t = \tau^2(n)$ is τ^2-bounded while the test generation complexity for t-time-bounded testable circuits with $t = \tau(n)$ and t-time-bounded validity-identifiable circuits with $t = \tau(n)$ is τ-equivalent.

A state-shiftable finite state machine [11] is a machine that possesses

C1. transfer sequences of length at most $[\log_2 m]$ to carry the machine from state s_0 to state s_i for all i, and

C2. distinguishing sequences of length $[\log_2 m]$, which are arbitrary input sequences consisting of 2 input symbols, where m denotes the number of states.

A sequential circuit that is realized from the SSFSM is called SSFSM realization. In this section, we introduce two easily testable classes of state-shiftable finite-state-machine (SSFSM) realizations, namely two-column SSFSM realizations with observable shifting logic (2COS-SSFSM) and two-column distributive SSFSM realizations (2CD-SSFSM). We address the test generation complexity for these classes with SAFs and PDFs, and the relationship between the test generation problems. We assume the slow-fast-slow clock and thus the circuit under test is fault-free during state justification and state differentiation for PDFs. By this assumption, we hypothesize that their test generation for PDFs is easier or equivalent to the test generation for SAFs.

Definition 6.5. *Two-column SSFSM realizations with observable shifting logic (2COS-SSFSM) is an SSFSM realizations that satisfies the following conditions:*

C1. There exists a two-column submachine of SSFSM of degree m, where $m = O(n)$ and n is the size of the 2COS-SSFSM. Let the the input symbols of the two-column be denoted by ϵ_0 and ϵ_1.

C2. Let C_0 and C_1 denote the input combinations (cubes) of ϵ_0 and ϵ_1, respectively, after the input assignments. The logic that is equivalent to $C_0 + C_1$ is called shifting logic and is a fanout of each next state function D_i and the output O_{ss} of SSFSM, where $1 \leq i \leq m-1$. The shifting logic S_L is made observable.
$S_L = C_0 + C_1$
$D_0 = C_0 \ OR \ F_0$
$\vdots$
$D_i = (C_0 + C_1) \ AND \ Q_{i-1} \ OR \ F_i$

$\vdots$

$D_{m-1} = (C_0 + C_1)$ *AND* Q_{m-2} *OR* F_{m-1}

$O_{ss} = (C_0 + C_1)$ *AND* Q_{m-1} *OR* F_{Oss}

Gate sharing is permitted during the synthesis. A OR B (resp. A AND B) means both logics are ORed (resp. ANDed) together. F_0, F_i, F_{m-1} *and* F_{Oss} *are* 0 *and independent of states under the input cubes contained by both* $\bar{C}_0$ *and* $\bar{C}_1$. *Figure 8 shows the general block diagram of a 2COS-SSFSM.*

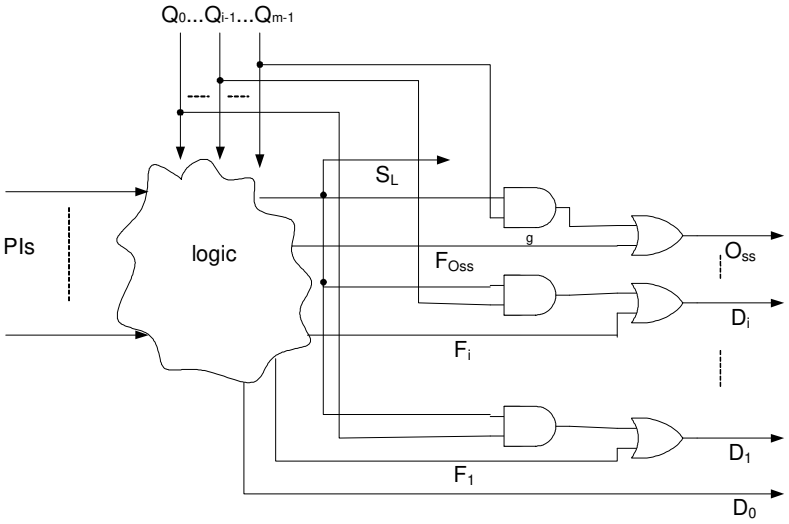

Figure 8: General block diagram of a two-column SSFSM realization with observable shifting logic.

Definition 6.6. *Distributive SSFSM is a two-column SSFSM with different pairs of input symbols for each state. Let the input symbols of two-column for state* s_j *be denoted by* $\gamma_0(s_j)$ *and* $\gamma_1(s_j)$, *respectively. Let* ϵ_0 *and* ϵ_1 *denote the input symbols of a two-column SSFSM, which has same degree with the distributive SSFSM. For each* j, $\delta(\epsilon_0, s_j) = \delta(\gamma_0(s_j), s_j)$ *and* $\delta(\epsilon_1, s_j) = \delta(\gamma_1(s_j), s_j)$.

Definition 6.7. *Two-column distributive SSFSM is SSFSM realizations that fulfills the following conditions:*

C1. There exists a two-column submachine of SSFSM of degree m, *where* $m = O(n)$ *and* n *is the size of the 2COS-SSFSM. Let the the input symbols of the two-column be denoted by* ϵ_0 *and* ϵ_1.

C2. There exists a distributive submachine of SSFSM over the columns other than those of ϵ_0 *and* ϵ_1. *The number of columns is* $2^{N-1} + 2$ *where* N *is an integer.*

C3. There exists an input symbol c *of the distributed submachine of SSFSM and a state* s_j *for* $0 \leq j \leq m-1$ *such that* $s_k = \delta(c, s_j)$ *and* $s_k \neq \delta(\epsilon_0, s_j)$, $s_k \neq \delta(\epsilon_1, s_j)$ *for* $k \neq j$ *and* $0 \leq k \leq m-1$.

C4. Let C_0 *and* C_1 *denote the input combinations of* ϵ_0 *and* ϵ_1 *respectively after the input assignment.* C_0 *and* C_1 *are two-bit assignments, one bit of which is different to each other. E.g.* $C_0 = ab'$ *and* $C_1 = ab$. *The similar bit of* C_0 *and* C_1 *is complement to other input*

combinations.
$SHIFT = C_0 + C_1$
$D_0 = C_0 \ OR \ F_0$
$\vdots$
$D_i = (C_0 + C_1) \ AND \ Q_{i-1} \ OR \ F_i$
$\vdots$
$D_{m-1} = (C_0 + C_1) \ AND \ Q_{m-2} \ OR \ F_{m-1}$
$O_{ss} = (C_0 + C_1) \ AND \ Q_{m-1} \ OR \ F_{Oss}$
Gate sharing is permitted during the synthesis. A OR B (resp. A AND B) means both implicants are ORed (resp. ANDed) together. F_0, F_i, F_{m-1} *and* F_{Oss} *are* 0 *and independent of states under the input cubes contained by both* $\bar{C}_0$ *and* $\bar{C}_1$.

Figure 9 shows the general block diagram of a 2CD-SSFSM. The following discusses the test

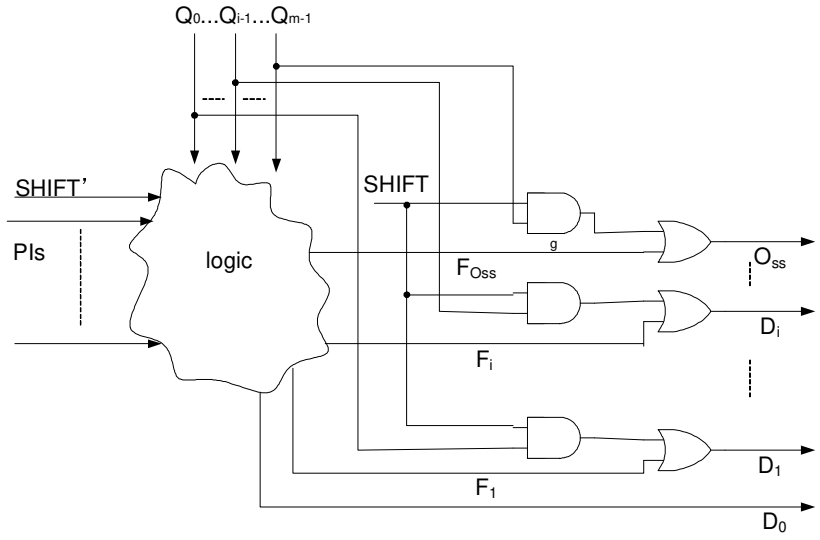

Figure 9: General block diagram of a two-column distributive SSFSM realization.

generation complexity for SAFs and PDFs.

6.2 Test Generation Complexity for Stuck-At Faults

Theorem 6.1. *The test generation complexity for two-column SSFSM realizations with observable shifting logic with SAFs is equivalent to the test generation complexity for combinational circuits with SAFs, which is* τ*-equivalent.*

Proof. In the following, several cases of faults are discussed. For each case, first the excitation state is derived. The state justification sequence is an input sequence consisting of ϵ_0 and ϵ_1 with length at most $m - 1$. If the fault is activated and propagates to one of the flip-flops before the circuit reaches the excitation state, the current state is made an excitation state.
Faults that is in the fanin cone of S_L
Since shifting logic S_L is observable, all the faults propagate to S_L are detectable.
Faults in the fanout-free region
For each testable fault f in the fanout-free region, it is guaranteed to be detectable without fault

masking during the shifting operation once the fault effect propagates to a flip-flop. Let the fault effect denoted by $\bar{d}$ that propagates to Q_h after the SAF is excited where $0 \leq h \leq m-1$.

$$D_{h+1} = S_L Q_h + F_{h+1}$$

For $S_L = 1$ during shifting operation,

$$D_{h+1} = \bar{d} + F_{h+1}$$

Note that no other fault effects propagate to F_{h+1} as f is in the fanout-free region and F_{h+1} has a fault-free value 0 during the shifting operation ($S_L = 1$). Therefore $D_{h+1} = \bar{d}$
The fault effect is propagated to $D_{h+2}, D_{h+3}, ..., D_{m-1}$ and then output O_{ss} for m is the degree of SSFSM. For example, the output of AND gate g is in fanout-free region (Figure 9).
Faults in fanout region other than stems Q_k
In generating tests for other faults which are in fanout region, we can assume the shifting operation is always working for S_L is observable. Let's discuss the faults in the fanout region other than those at the stems of Q_k for $0 \leq k \leq m-1$. During the phase of derivation of SAF excitation state, any input cubes contained by C_0 or C_1 are prioritized as the input pattern to excite the fault f. If one of them is a test, the fault effect that propagates to a flip-flop must be $\bar{d}$ as discussed in the following.

$$D_i = (C_0 + C_1) \text{ AND } Q_{i-1} \text{ OR } F_i$$

F_i has fault-free value 0 during shifting operation. In addition, shifting logic S_L and Q_{i-1} are fault free. Therefore the fault effect propagates to F_i must be $\bar{d}$ after the SAF is excited if there exists an input cube that is contained by C_0 or C_1 and excites the fault f. During differentiation,

$$\begin{aligned} Q_i &= \bar{d} \\ D_{i+1} &= \bar{d} + F_{i+1} \end{aligned}$$

Since this is done by shifting operation where $S_L = 1$ and each stem of Q_k for $0 \leq k \leq m-1$ is fault-free, if the fault f is activated again during differentiation, it will propagate to F_{i+1} as $\bar{d}$, which has the same polarity as the fault effect of SAF in the derivation of excitation state. Therefore, fault masking does not happen during differentiation. In the case where no input cubes that are contained by C_0 or C_1 excite the fault, the fault is not excited during the phase of state differentiation and thus fault masking does not occur.
Faults at the stems of Q_k
For the faults at the stems of Q_k where $0 \leq k \leq m-1$, each fault change only one bit of the current state in the flip-flops without changing the logic of the circuit, thus we still can observe the partial state of the excitation state from the most significant bit to the faulty bit after at most $m-1$ clock cycles during state differentiation.
Let T_E, T_J and T_D denote the running time of SAF excitation, justification and differentiation respectively.

$$\begin{aligned} T_{2COS}^{SA}(n) &= T_E + T_J + T_D \\ &= \tau(n) + O(m-1) + O(m-1) \\ &= \tau(n) + O(n) + O(n) \text{ for m=O(n)} \\ &= \Theta(\tau(n)) \end{aligned}$$

□

Theorem 6.2. *The test generation complexity for two-column distributive SSFSM realizations with SAFs is τ^2-bounded.*

Proof. The proof is similar to the proof for Theorem 6.1 by considering the faults at SHIFT instead of the faults in the fanin cone of S_L.
Faults at SHIFT
Looking into the case where the fault is at the stem of SHIFT, the shifting operation of the circuit fails. However, the distributive shifting operation is intact. First, the SAF is excited at running time $\tau(n)$. To differentiate a pair of fault-free and faulty states after the SAF is excited, the fault effect at a flip-flop is propagated to the output O_{ss} by searching the input sequence on its iterative logic array of size at most $m-1$. Since $m = O(n)$, the running time of the differentiation is $O(\tau^2(n))$. For s-a-1 at the stem of SHIFT, it is obviously easy to test since during differentiation (SHIFT=1), the fault is not activated again.
Let T_E, T_J and T_D denote the running time of SAF excitation, justification and differentiation. Therefore,

$$\begin{aligned} T^{SA}_{2CD}(n) &= T_E(n) + T_J + T_D \\ &= \tau(n) + O(m-1) + O(\tau((m-1)n)) \\ &= \tau(n) + O(n) + O(\tau^2(n)) \text{ for } m = O(n) \\ &= O(\tau^2(n)) \end{aligned}$$

□

However, we cannot conclude that the test generation complexity for two-column distributive SSFSM realizations with SAFs is not τ-equivalent although it seems to be correct.

Conjecture 6.1. *The test generation complexity for two-column distributive SSFSM realizations with SAFs is not τ-equivalent.*

6.3 Test Generation Complexity for Path Delay Faults

Definition 6.8. *Let P and P' denote a path in a given cyclic sequential circuit $\mathcal{S}^{\mathcal{C}}$ and the corresponding path in its combinational part c. A duplex combinational circuit $C^D_P(\mathcal{S}^{\mathcal{C}})$ for P (Figure 10) of a cyclic sequential circuit $\mathcal{S}$ can be obtained by the following transformation:*

S1. Perform the single-path-leaf transformation for P' on c. The inputs of c corresponding to the outputs of the flip-flops in $\mathcal{S}^{\mathcal{C}}$ are called the pseudo inputs while the outputs of c corresponding to the inputs of the flip-flops in $\mathcal{S}^{\mathcal{C}}$ are called the pseudo outputs. The resulting single-path leaf-dag is denoted by $c^{LD}_{P'}$.

S2. Duplicate $c^{LD}_{P'}$. The single-path leaf-dag $c^{LD}_{P'}$ and its duplicate are named as the first partial circuit c_1 and the second partial circuit c_2.

S3. Connect the pseudo outputs of c_1 to the corresponding pseudo inputs of c_2 to form an iterative logic array of single-path leaf-dag of size 2. The new connections between c_1 and c_2 are called pseudo interconnections and a pseudo interconnection is labeled as QD_i while a resulting pseudo input and pseudo output are labeled as Q_i and D_i respectively, corresponding to flip-flop i in $\mathcal{S}^{\mathcal{C}}$. Note that the path P in $\mathcal{S}^{\mathcal{C}}$ corresponds to two segments S_{c1} and S_{c2} in $C^D_P(\mathcal{S}^{\mathcal{C}})$. A primary input and a primary output of c_1 is denoted by I_{1j} and O_{1k}, respectively while a primary input and a primary output of c_2 is denoted by I_{2j} and O_{2k}.

Definition 6.9. *Let $P\uparrow$ denote a rising PDF in a given cyclic sequential circuit $\mathcal{S}^{\mathcal{C}}$. A duplex combinational circuit $C_P^D(\mathcal{S}^{\mathcal{C}})$ for P can be transformed into a path-rising-smooth duplex circuit(resp. path-falling-smooth duplex circuit) $C_S^{PRS}(\mathcal{S}^{\mathcal{C}})$ (resp. $C_S^{PFS}(\mathcal{S}^{\mathcal{C}})$) for the corresponding segment S_{c2} by the following procedure:*

S1. Let Q_{OR} (resp. Q_{AND}) denote the OR gates (resp. AND gates) along S_{c2} corresponding to $P\uparrow$ (resp. $P\downarrow$). A gate may have no parity, 0, 1 or both parities. A side-input to an OR gate (resp. AND gate) in Q_{OR} (resp. Q_{AND}) has parity 1 (resp. 0). Perform a reverse topological traversal from the transitive fanout of all pseudo interconnections, to determine the parity of all gates along the side-paths to S_{c2}. The parity is complemented across a NOT gate. If some fanouts of a gate have parity 1 and others have parity 0, the gate is assigned both parities.

S2. Duplicate gates so that each resulting gate has parity of either nothing, 0 or 1 but not both.

S2.1. Traversing from flip-flop or primary output g_m on P, for each gate h_j with a parity (parities) and with a successor gate that is off path and without parity, h_j and the connections of its immediate predecessor gates are duplicated once and its duplicate h'_j has no parity. For each immediate successor gate h_{j+1} of h_j that has no parity, the connection from h_j to h_{j+1} is replaced by the connection from h'_j to h_{j+1}.

S2.2. Traversing from flip-flop or primary output g_m, each gate h_j with both parities and the connections to its immediate predecessor gates are duplicated once and assigned parity 1 while its duplicate h'_j is assigned parity 0. For each immediate successor gate h_{j+1} of h_j that has parity 0 (1 if there is an inversion between h_j and h_{j+1}), the connection from h_j to h_{j+1} is replaced by the connection from h'_j to h_{j+1}.

S3. Insert to the fanout branch of a second circuit primary input I_{2j} a segment-transition-smoother STS(I_{2j}, I_{1j}) if the fanout branch has an immediate gate with parity 0 or 1. At the fanout branch of a pseudo interconnection QD_i, insert a segment transition-smoother STS(QD_i, Q_i) if the QD_i has an immediate gate with parity 0 or 1.

Lemma 6.1. *$< v_1, v_2 >$ is an input sequence that robustly excites a PDF $P\uparrow$ (resp. $P\downarrow$) of a sequential circuit $\mathcal{S}^{\mathcal{C}}$ in present state s_1 if and only if $s_1 + v_1 + v_2$ is a test for SA0 at the S-edge of S_{c2} with an input constraint of 0 at the S-edge of S_{c1} in the corresponding path-rising-smooth duplex circuit $C_S^{PRS}(\mathcal{S}^{\mathcal{C}})$.*

Proof. **If part:** $s_1 + v_1 + v_2$ is a test for SA0 at the S-edge of S_{c2} with an input constraint 0 at the S-edge of S_{c1}. In the fault free case, S-edge of S_{c1} and S-edge of S_{c2} have different values under $s_1 + v_1 + v_2$. This means $< v_1, v_2 >$ initializes the corresponding $P\uparrow$. The value at the ending points of S_{c2} and S_{c1} are 0 and 1 respectively under $s_1 + v_1 + v_2$. All the side-inputs of the gates along S_{c2} are at the non-controlling values. Thus, all the side-input of gates along P are at the non-controlling value under v_2. Segment transition-smoother guarantees that the transition at a flip-flop or a primary input does not propagate to the side-inputs of OR gates along P under $< v_1, v_2 >$. Therefore, $< v_1, v_2 >$ robustly excites $P\uparrow$.
Only If part: $< v_1, v_2 >$ robustly excites $P\uparrow$. All side inputs of gates along P are at the non-controlling values. The value at the S-edge of S_{c2} is different from that at the S-edge of S_{c1}. This excites the SA0 at the S-edge of S_{c2} and put a constraint 0 to the S-edge of S_{c1}. According to the definition of robust PDF, the side inputs of gates along S_{c2} are at the non-controlling value. This satisfies the test condition. Therefore, $s_1 + v_1 + v_2$ is a test for SA0 at the S-edge of S_{c2} with an input constraint of 0 at the S-edge of S_{c1}. □

Lemma 6.2. *$< v_1, v_2 >$ is an input sequence that non-robustly excites a PDF $P\uparrow$ (resp. $P\downarrow$) of a sequential circuit $\mathcal{S}^{\mathcal{C}}$ in present state s_1 if and only if $s_1 + v_1 + v_2$ is a test for SA0 at the S-edge of S_{c2} with an input constraint of 0 at the S-edge of S_{c1} in the corresponding path-rising-smooth duplex combinational circuit $C_S^{PRS}(\mathcal{S}^{\mathcal{C}})$.*

Proof. **If part:** $s_1 + v_1 + v_2$ is a test for SA0 at the S-edge of S_{c2} with an input constraint 0 at the S-edge of S_{c1}. In the fault free case, S-edge of S_{c2} and S-edge of S_{c1} have the different values under $s_1 + v_1 + v_2$. This initializes the $P\uparrow$. The value at the ending points of S_{c2} and S_{c1} are 0 and 1 respectively under $s_1 + v_1 + v_2$. All the side-input of gates along P are at the non-controlling value. Therefore, $< v_1, v_2 >$ non-robustly excites $P\uparrow$.
Only If part: $< v_1, v_2 >$ non-robustly excites $P\uparrow$. All the side inputs of gates along P are at the non-controlling values. The value at the S-edge of S_{c2} is different from that at the S-edge of S_{c1}, which is 1 and 0 respectively. This excites the SA0 at the S-edge of S_{c2} and put a constraint 0 to the S-edge of S_{c1}. According to the definition of PDF, the side inputs of gates along S_{c2} are at non-controlling value. This satisfies the test condition. Therefore, $s_1 + v_1 + v_2$ is a test for SA0 at the S-edge of S_{c2} with an input constraint of 0 at the S-edge of S_{c1}. □

Lemma 6.3. *The derivation of PDF excitation state is equivalent to the test generation for path-rising-smooth duplex combinational circuits with SAFs at S-edges, which is τ-bounded.*

Proof. We showed a pseudo-transformation that transforms the kernel of a given cyclic sequential circuit so that the derivation of PDF excitation state can be done by combinational test generation. To activate a PDF in a given sequential circuit $\mathcal{S}^{\mathcal{C}}$, for each PDF

S1. Derive the duplex combinational circuit $C^D(\mathcal{S}^{\mathcal{C}})$.

S2. Derive the path-rising-smooth duplex circuit $C_S^{PRS}(\mathcal{S}^{\mathcal{C}})$ (for robust test).

S3. Perform the combinational test generation for SA0 at the S-edge of S_{c2} with an input constraint 0 at the S-edge of S_{c1}. Let $s_1 + v_1 + v_2$ denote the test obtained.

S4. Transform $s_1 + v_1 + v_2$ into an input sequence $< v_1, v_2 >$ for the PDF activation.

Based on Lemma 6.1-6.2, the derivation of PDF excitation state can be modeled by the test generation for SAFs. Let $T_D(N_D)$, $T_{PRS}(N_{PRS})$, $T_c^{SAF}(N_c^{SAF})$ and $T_P(N_P)$ denote the time complexity of the duplex combinational circuit derivation, the path-rising-smooth duplex circuit derivation, the combinational test generation for SAFs and the two-pattern test transformation. Let n denote the size of a given cyclic sequential circuit $\mathcal{S}^{\mathcal{C}}$. To derive a duplex combinational circuit, it takes $O(n^2)$ according to Definition 6.8. After the derivation, the size of the resulting circuit is at most $4n$. The procedures of transforming a C^D into a C_S^{PRS} involve only the first partial circuit C_1 of C^D. The process takes $O(n^2)$ as explained in Definition 6.9. The size of the resulting circuit is at most $8n$. Therefore, the time complexity of the PDF excitation is

$$\begin{aligned} T_E^{PD} &= T_D(N_D) + T_{PRS}(N_{PRS}) + O(T_c^{SAF}(N_c^{SAF})) + T_P(N_P) \\ &= O(n^2) + O(4n^2) + O(\tau(8n)) + O(n) \\ &= O(\tau(n)). \end{aligned}$$

□

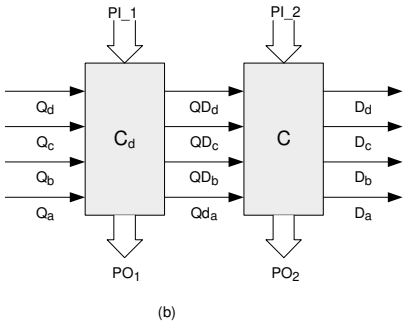

Figure 10: A duplex combinational circuit.

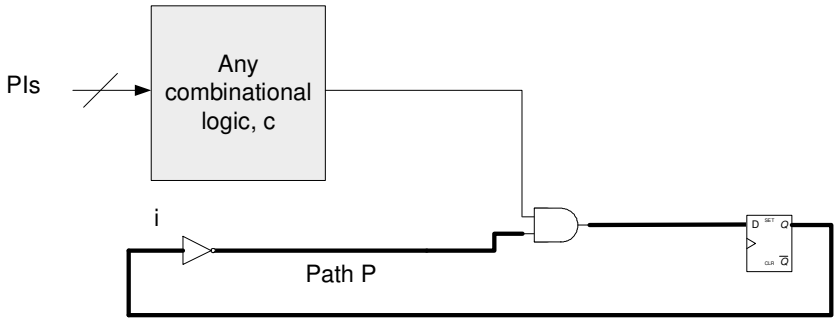

Figure 11: A cyclic sequential circuit S_Z.

Definition 6.10. *A cyclic sequential circuit S_Z has a fanout-inverter-free single-path leaf-dag with an inverter at the primary input on P as its combinational kernel. The primary input on P is connected to the output of flip-flop while the primary output on P is connected to the input of flip-flop as shown in Figure 11.*

Lemma 6.4. *v is a test for SAF f in a combinational circuit C if and only if $< v, v >$ excites the PDF $P\uparrow$ or $P\downarrow$ in the corresponding cyclic sequential circuit S_Z with $c = C \oplus C_f$.*

Proof. **If part:** Under $< v, v >$, the side-input of AND gate is at the stable 1. In other words, under vector v, the side input of AND gate is 1, which implies logic c is satisfied.
Only If part: Under v, the side-input of AND gate is 1. Therefore, the transition along P can be propagated to the flip-flop and thus the PDF is excited under $< v, v >$. □

Theorem 6.3. *The derivation of PDF excitation state is τ-equivalent.*

Proof. To prove that the derivation of PDF excitation state is τ-equivalent, in addition to Lemma 6.3, it is sufficient to prove that the test generation for combinational circuits with SAFs can be transformed into the derivation of PDF excitation state of cyclic sequential circuits. Therefore, Lemmas 6.3 and 6.4 prove it. □

Theorem 6.4. *The test generation complexity for two-column SSFSM realizations with observable shifting logic with PDFs under slow-fast-slow clock is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

Proof. In deriving PDF excitation state, the input sequence $< v_1, v_2 >$ is derived. Let the excitation state be denoted by s_e. According to Theorem 6.3, the running time of deriving PDF excitation state is $\Theta(\tau(n))$, which is reducible to the derivation of excitation state for an SAF. Since slow-fast-slow clock is used, there is no fault effect during justification and differentiation. Therefore, any excitation state is justifiable by an input sequence consisting of ϵ_0 and ϵ_1 with length at most $m-1$ while a pair of faulty and fault-free next states after the derivation of PDF excitation state can be differentiated by any input sequence consisting of ϵ_0 and ϵ_1 with length at most $m-1$, where m is the degree of SSFSM. Obviously the test generation for PDFs is τ-equivalent. □

However, it is still unsolved for the case under rated clock.

Open Problem 6.1. *Is the test generation complexity for two-column SSFSM realizations with observable shifting logic with PDFs under rated clock equivalent to the test generation for two-column SSFSM realizations with observable shifting logic with SAFs, which is τ-equivalent?*

Theorem 6.5. *The test generation complexity for two-column distributive SSFSM with PDFs under slow-fast-slow clock is equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent.*

Proof. Same as the proof of PDF test generation in Theorem 6.4. □

We also have not yet solved the PDF test generation complexity of the two-column distributive SSFSM realizations under rated clock.

Open Problem 6.2. *Is the test generation complexity for two-column distributive SSFSM realizations with PDFs under rated clock equivalent to the test generation complexity for combinational circuits with SAFs, which is τ-equivalent?*

The test generation for 2COS-SSFSM with PDFs under slow-fast-slow clock is equivalent to that with SAFs, which is τ-equivalent. The test generation for 2CD-SSFSM with PDFs under slow-fast-slow clock is τ-equivalent while that with SAFs is τ^2-bounded. In other words, if Conjecture 6.1 is proved, 2CD-SSFSM is a class, the test generation complexity for PDFs under slow-fast-slow clock is less than that for SAFs.

7 Conclusion

The time complexity and the relationships between the test generation problem for several existing classes of circuits with stuck-at and path delay faults have been described in this paper. The test generation for internally balanced sequential circuits with SAFs and PDFs under rated clock and slow-fast-slow clock is equivalent to the test generation for combinational circuits with SAFs. On the other hand, the test generation for the acyclic sequential circuits with SAFs and PDFs under slow-fast-slow clock are τ^2-bounded. It is shown that under TEM at slow-fast-slow clock the test generation for PDFs is not τ-equivalent. The test generation for two-column SSFSM realizations with observable shifting logic under slow-fast-slow clock and that for SAFs are equivalent to the test generation for combinational circuits with SAFs while for two-column distributive SSFSM realizations with PDFs under slow-fast-slow clock, its test generation complexity is τ-equivalent but that with SAFs is τ^2-bounded. The test generation for two-column distributive SSFSM realizations with SAFs seems to be not τ-equivalent so we put it as a conjecture. If it is proved, two-column distributive SSFSM realizations will be the class of circuits that has the test generation complexity for PDFs less than the test generation complexity for SAFs. The test generation for acyclic

sequential circuits and cyclic sequential circuits with PDFs is discussed under the assumption of slow-fast-slow clock. The similar discussion under rated clock remain important open problems. The solutions will contribute to the ATPG and DFT development.

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