Some τ-Equivalent Classes of Sequential Circuits

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Abstract

Based on τ^k notation, the test generation complexity of several existing classes of sequential circuits has been reconsidered. Some classes of easily testable sequential circuits that cover some cyclic sequential circuits have also been introduced. These classes include length-bounded testable circuits, time-bounded testable circuits and time-bounded validity-identifiable circuits. In this paper, we introduce two classes of sequential circuits, state-shiftable finite state machine realizations and counter-cycle one-hot design realizations, which are subclasses of k-time-bounded testable circuits and k-time-bounded validity-identifiable circuits, respectively, where k is $\tau(n)$ and n is the size of the circuits .

Keywords: *τ^k notation, counter-cycle one-hot design, state-shiftable finite state machine.*

1. Introduction

It has been theoretically proved that the test generation problem is NP-complete. However, empirical observation shows that the combinational test generation complexity seems to be $O(n^r)$, for some constant r where n is the size of the circuit. It has been proved that the test generation problem of balanced sequential circuits, internally balanced sequential circuits and strongly balanced sequential circuits can be reduced to the combinational test generation problem. The test generation complexity of acyclic sequential circuits seems to be near to combinational test generation complexity but the problem may not be reducible to combinational test generation problem.

In order to clarify the test generation complexity, we introduced τ^k notation in [1]. Let $T_\alpha(n)$ be the test generation complexity of a given class α of circuits. The class α is τ^k-equivalent if $T_\alpha(n)=\Theta(\tau^k(n))$ and τ^k-bounded if $T_\alpha(n)=O(\tau^k(n))$, where $k>0$ and n is the size of the circuits. Based on τ^k notation, we concluded that balanced sequential circuits, strongly balanced sequential circuits and internally balanced sequential circuits are τ-equivalent. All circuits belong to these classes are acyclic. On the other hand, we identified three classes of easily testable sequential circuits that cover some cyclic sequential circuits. In these classes, backtracks between state justification, fault propagation and derivation of excitation state do not occur. The time complexity of derivation of excitation state is always τ-equivalent and the time complexity of justification and state differentiation are τ^2-bounded, τ-equivalent or less. These classes of easily testable sequential circuits include length-bounded testable circuits, time-bounded testable circuits and time-bounded validity-identifiable circuits. The test generation complexity for the k-length-bounded testable circuits is τ^2-bounded if the parameter k is O(n) while the test generation complexity for k-time-bounded testable circuits and k-time-bounded validity-identifiable circuits is τ-equivalent (τ^2-bounded) if the parameter k is $\tau(n)$ ($\tau(n^2)$).

In this paper, we identify state-shiftable finite state machine realizations as a subclass of k-time-bounded testable circuits and counter-cycle one-hot design realizations as a subclass of k-time-bounded validity-identifiable circuits, where k is $\tau(n)$. In Section 2, we introduce the state-shiftable finite state machine realizations. In Section 3, another class called counter-cycle one-hot design realizations is presented. In Section 4, the conclusion is presented.

2. State-Shiftable Finite State Machine Realizations

A state-shiftable finite state machine [2] is a machine that possesses

1. transfer sequences of length at most $[\log_2 m]$ to carry the machine from state s_0 to state s_i for all i, and
2. distinguishing sequences of length $[\log_2 m]$, which are arbitrary input sequences consisting of 2 input symbols, where m denotes the number of states.

A sequential circuit that is realized from the state-shiftable finite state machine (FSM) is called state-shiftable finite state machine (FSM) realization.

Theorem 1: State-shiftable FSM realizations is τ-equivalent if the following conditions are satisfied.

1. The FSM contains a 2-column submachine equivalent to a binary shift register;
2. The output logic sub circuit OL' with input symbols ε_0 and ε_1 is separate from other logic sub circuits; and

3. All the next state logic sub circuits with input symbols ε_0 and ε_1 are separate from each other, where input symbols ε_0 and ε_1 shift bit 0 and 1, respectively into the least significant bit or LSB of the next state.

Proof: Let m denotes the number of state variables, where q_{m-1} is the most significant bit or MSB while q_0 is the least significant bit or LSB and the shift operation is from bit 0 to bit m-1. Let's consider two types of single-faults in a given state-shiftable FSM realization, i.e. single-faults in output logic sub circuit OL' with input symbols ε_0 and ε_1 and single-faults in logic sub circuits other than OL'.

1. A single-fault in the output logic sub circuit OL' with input symbols ε_0 and ε_1.

To generate a test sequence for a single-fault in OL', firstly an excitation state s_e is derived to activate the fault and propagate it to the primary output as shown in Figure 1(a).

$\lambda_f(s_e,\varepsilon)\neq\lambda(s_e,\varepsilon)$ where λ_f means the faulty logic for OL'.

Secondly, s_e is justified by applying transfer sequence of length at most $[\log_2 m]$, which are consisting of input symbols ε_0 and ε_1, where m is the number of states. For example, if s_e=111, transfer sequence of length at most 3, which are consisting of $\varepsilon_1\varepsilon_1\varepsilon_1$, is necessary to transfer from state 000 to s_e as illustrated by Figure 1(b). If the fault is detected before s_e is reached, the present state becomes the excitation state s_e. Note that state differentiation process is not required.

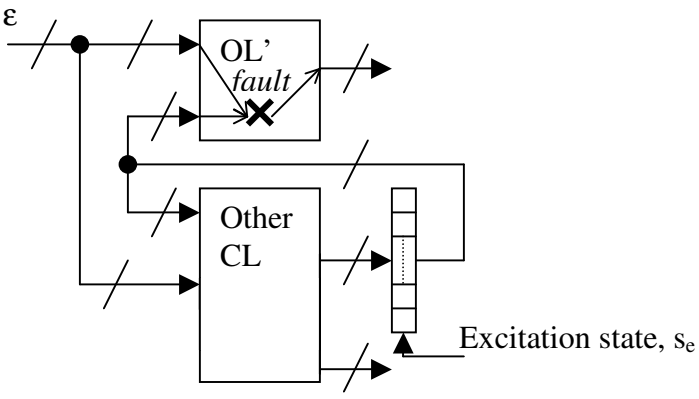

Figure 1(a). Derivation of excitation state.

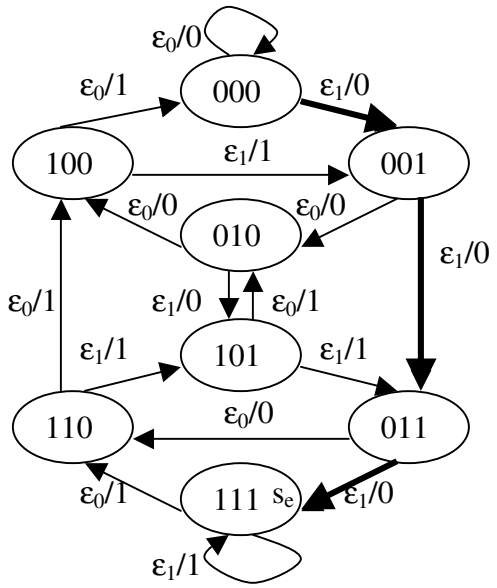

Figure 1(b). State justification.

2. A single-fault in a logic sub circuit other than OL'.

To generate a test sequence for a single-fault in a logic sub circuit other than OL', firstly an excitation state s_e is derived to activate the fault and propagate it to a flip-flop or primary output. Secondly, s_e is justified by applying transfer sequence of length at most $[\log_2 m]$, which

are consisting of input symbols ε_0 and ε_1, where m is the number of states (Figure 1(b)). If the fault is propagated to a primary output or a flip-flop before s_e is reached, the present state becomes the excitation state s_e. Let s_i and s_j be a fault-free state and faulty state, respectively, resulted from the derivation of excitation state and state justification. Lastly, the pair of states (s_i,s_j) are differentiated by applying a distinguishing sequence of length $[\log_2 m]$, which is an arbitrary input sequence consisting of input symbols ε_0 and ε_1.

Let T_E, T_J and T_D denote the test generation complexity for the derivation of excitation state, state justification and state differentiation.

$T_E(n)=\tau(n)$;
$T_J(n)=O(n\bullet\log m)=O(n^2)$ for log m=O(n); and
$T_D(n)=O(n\bullet\log m)=O(n^2)$ for log m=O(n).

Consequently, the test generation complexity of the state-shiftable FSM realizations is

$$\begin{aligned} T_{SSFSM}(n) &\le T_E(n)+T_J(n)+T_D(n) \\ &= \tau(n)+O(n^2)+O(n^2) \\ &= \tau(n). \end{aligned}$$

State-shiftable FSM realizations is τ-equivalent if the following conditions are satisfied.

1. The FSM contains a 2-column submachine equivalent to a binary shift register;
2. The output logic sub circuit with input symbols ε_0 and ε_1 is separate from other logic sub circuits; and
3. All the next state logic sub circuits with input symbols ε_0 and ε_1 are separate from each other.

Note that full scan designed circuits is a sub-class of the easily testable state-shiftable FSM realizations where the next state logic sub circuits with input symbols ε_0 and ε_1 are multiplexers of the scan flip-flops and the output logic sub circuit with ε_0 and ε_1 is logic sub circuit for the output of the last scan flip-flop in the scan chain.

3. Counter-Cycle One-Hot Design Realizations

Let $s_{i,1}, s_{i,2},\ldots, s_{i,Pi}$ denote the set of all distinct states (codeword states) that have s_i, as a possible next state. For each such state $s_{i,j}$, let $x_{(i,j),1}, x_{(i,j),2},\ldots, x_{(i,j),N(j)}$ be all input combinations that have $s_{i,j}$ as initial state and s_i as the final state. N(j) is the number of the input combinations. Then, the next-state equation (or function) for d_i that defines s_i in the one-hot assignment is

$$\begin{aligned} d_i = {} & q_{i,1}\bullet(x_{(i,1),1}+x_{(i,1),2}+\ldots+x_{(i,1),N(1)}) \\ & +q_{i,2}\bullet(x_{(i,2),1}+x_{(i,2),2}+\ldots+x_{(i,2),N(2)}) \\ & +q_{i,3}\bullet(x_{(i,3),1}+x_{(i,3),2}+\ldots+x_{(i,3),N(3)}) \\ & \ldots \\ & +q_{i,Pi}\bullet(x_{(i,Pi),1}+x_{(i,Pi),2}+\ldots+x_{(i,Pi),N(Pi)}) \end{aligned} \quad (1)$$

Let $X_{(i,j)}$ be a set consists of all input combinations that have $s_{i,j}$ as an initial state and s_i as the final state.

$$X_{(i,j)} = \{x_{(i,j),p} \mid 1 \le p \le N(j)\}$$

Let $x_{i,1}/z$, $x_{i,2}/z$, …, $x_{i,U(j)}/z$, be all outgoing transition labels from state s_i that require setting z=1. U(j) denotes the number of input combination. Then, summing over all states s_1, s_2…, s_{Vi} with z activated at least once in an outgoing transition, we obtain

$$\begin{aligned} z &= q_1 \bullet (x_{1,1} + x_{1,2} + ... + x_{1,U(1)}) \\ &+ q_2 \bullet (x_{2,1} + x_{2,2} + ... + x_{2,U(2)}) \\ &+ q_3 \bullet (x_{3,1} + x_{3,2} + ... + x_{3,U(3)}) \\ &... \\ &+ q_{Vi} \bullet (x_{Vi,1} + x_{Vi,2} + ... + x_{Vi,U(Vi)}) \end{aligned} \qquad (2)$$

Lemma 1: For any one-hot design with codeword present state,
$X_{(i,j)} \bigcap X_{(h,j)} = \phi \quad if \quad s_{i,j} = s_{h,j} \quad and \quad s_i \neq s_h$

Proof: Let $X_{(i,j)} \bigcap X_{(h,j)} = X_{(ih,j)} \neq \phi \quad and \quad q_{i,j} = q_{h,j} = 1$. Note that $q_{i,j}$ and $q_{h,j}$ are outputs of same flip-flops. Let $x_{(ih,j),c} \in X_{(ih,j)}$ where $1 \le c \le |X_{(ih,j)}|$. From equation (1),

$d_i = 1 \quad and \quad d_h = 1 \quad at \quad x_{(ih,j),c}$, which contradicts with $s_i \neq s_h$.

Lemma 2: All the valid states of a resettable one-hot design realization are codeword states.

Proof: Let s_l be a next state of $s_{l,k}$ at input combination $x_{(l,k),c}$. Let the one-hot design realization is in present state $s_{l,k}$, which is a codeword state with bit $q_{l,k}$ ON. From Lemma 1, only one bit of next state is ON, that is d_l.

Lemma 2 implies that the next state is always a codeword state if the present state is a codeword state if the realization of a one-hot design is resettable.

Lemma 3: Let s_z denotes the state all bits OFF and s_i denotes a non-codeword state that is not s_z and s_k be a codeword state in a set S_1 that is a subset of codeword states $S_{codeword}$. Then,

$\delta(s_i, \varepsilon) = \bigvee_{s_k \in S_1} \delta(s_k, \varepsilon)$ if $s_i = \bigvee_{s_k \in S_1} s_k$, where $S_1 \subseteq S_{codeword}$.

Lemma 4: Let s_i be a non-codeword state. Let Z_k be the output combination generated by s_k and an input symbol ε. The output symbol Z_i generated by s_i and the input symbol ε, is

$Z_i = \bigvee_{Z_k = \lambda(s_k, \varepsilon)} Z_k$ if $s_i = \bigvee_{s_k \in S_1} s_k$, where $S_1 \subseteq S_{codeword}$.

Counter-cycle one-hot design realization satisfies the following conditions.

1. The number of codeword states is in O(n) and there exists a codeword checker of size O(n);
2. There exists an input symbol ε that strongly connects all codeword states accordingly in a counter-cycle such that
    a. the output function $\lambda(s_i,\varepsilon)=01$ if the state transition function $\delta(s_i,\varepsilon)=s_0$; and
    b. the output function $\lambda(s_i,\varepsilon)=10$ if the state transition function $\delta(s_i,\varepsilon)\in S_V-\{s_0\}$; and
3. Output logic sub circuit OL' with input symbol ε is separate from other logic sub circuits;
4. All the next state logic sub circuits with input symbol ε are separate from each other, and
5. The counter-cycle one-hot design realization is resettable, where $s_i,s_0\in S_V$, which is a set of all codeword states, s_0 is the initial state of the counter-cycle and n is the size of the counter-cycle one-hot design realization.

Theorem 2: Counter-cycle one-hot design realizations is τ-equivalent.

Proof: Let's assume the one-bit in each state of a given counter-cycle one-hot design realization is shifted 1 bit to the left for each transition and $s_0=0^{m-1}\cdot 1$ as in Figure 2, where m is the number of codeword states and 0^{m-1} means the concatenation of (m-1) 0's. Let's consider two types of single-faults in the counter-cycle one-hot design realization, i.e. single-faults in output logic sub circuit OL' with input symbol ε and single-faults in logic sub circuits other than OL'.

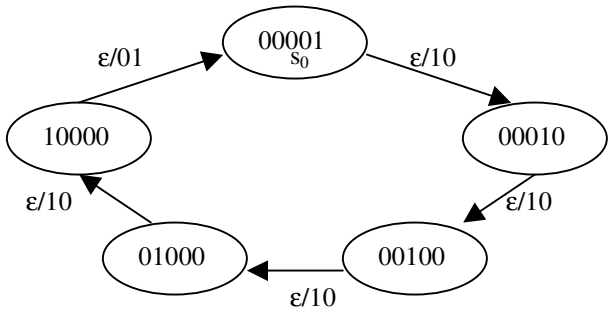

Figure 2. Counter-cycle in the one-hot design.

1. A single-fault in the output logic sub circuit OL' with input symbol ε.

To generate a test sequence for a single-fault in the output logic sub circuit OL', firstly an excitation state s_e is derived to activate the fault and propagate it to the primary output. The excitation state derived s_e is always a codeword state by embedding codeword checker in the counter-cycle one-hot design realization while excitation state is being derived. Secondly, s_e is justified by applying input sequence of length at most m, which are consisting of input symbol ε, where m is the number of codeword states. If the fault is detected before s_e is reached, the present state becomes the excitation state s_e. Note that the step of state differentiation is not required. For

example, if s_e is 00001 and the initial state of the circuit is 00010, then the justification sequence of length 4, consisting of εεεε is necessary as illustrated in Figure 3(a) and 3(b).

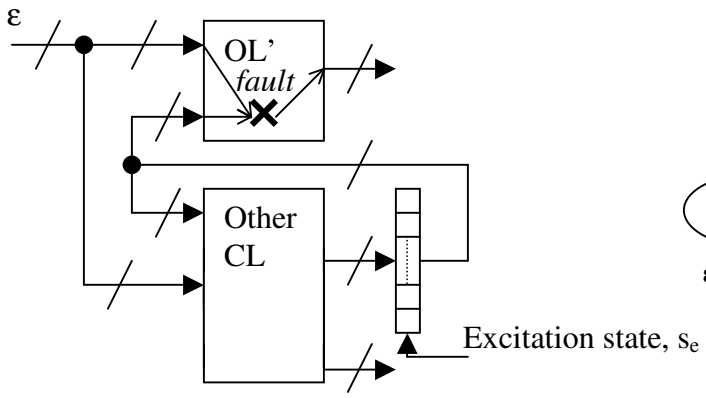

Figure 3(a). Derivation of excitation state.

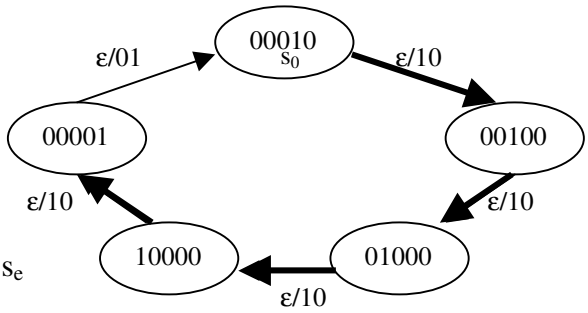

Figure 3(b). state justification.

2. A single-fault in a logic sub circuit other than OL'.

To generate a test sequence for a single-fault in a logic sub circuit other than OL', firstly an excitation state s_e are derived to activate the fault and propagate it to a flip-flop. Secondly, s_e is justified by applying input sequence of length at most m, which are consisting of input symbol ε, where m is the number of codeword states. If the fault is propagated to a primary output or a flip-flop before s_e is reached, the present state becomes the excitation state s_e. Let s_i and s_j be a fault-free state and faulty state, respectively, resulted from the derivation of excitation state. Based on lemma 3 and 4, if the one-bit in s_i is more significant than all the faulty bits in s_j, the fault is detected when the one-bit of s_i has been shifted during state differentiation and becomes the most significant bit. Let consider s_j is a faulty state with one faulty bit D'. For the case where the faulty bit D' in s_j is more significant than the one-bit in s_i, the pair of state (s_i,s_j) can be differentiated when the faulty bit D' has been shifted and becomes the most significant bit during state differentiation. If the fault effect D is propagated to a state bit during the derivation of excitation state, the fault effect is guaranteed to propagated to a primary output in the next time frame since all bits of output symbol $\lambda(s_z, \varepsilon)$ are zeros based on equation 2, where s_z denotes a state where all bits are zeros or OFF. Therefore, the pair of states (s_i,s_j) can be differentiated by applying input sequence of length at most m consisting of input symbol ε, where m denotes the number of the codeword states.

Let T_E, T_J and T_D denote the test generation complexity for the derivation of excitation state, state justification and state differentiation.

$T_E(n)=\tau(2\bullet n)= \tau(n)$;
$T_J(n)=O(n\bullet m)=O(n^2)$ for m=O(n); and
$T_D(n)=O(n\bullet m)=O(n^2)$ for m=O(n).

Consequently, the test generation complexity of the counter-cycle one-hot design realizations is

$$\begin{aligned} T_{CCOH}(n) &\le T_E(n)+T_J(n)+T_D(n) \\ &= \tau(n)+O(n^2)+O(n^2) \\ &= \tau(n). \end{aligned}$$

Counter-cycle one-hot design realizations is τ-equivalent.

4. Conclusion

State-shiftable finite state machine realizations has been identified as a subclass of k-time-bounded testable circuits where k is $\tau(n)$ and n is the size of the circuits if each FSM realization in this class satisfies the following conditions.

1. The FSM contains a 2-column submachine equivalent to a binary shift register;
2. The logics of all the next state functions with input symbols ε_0 and ε_1 are separate from each other; and
3. The output logic and next state logic are separate from each other.

Counter-cycle one-hot design realizations has also been identified as a subclass of k-time-bounded validity-identifiable circuits, where k is $\tau(n)$ and n is the size of the circuits. In other words, state-shiftable finite state machine realizations and counter-cycle one-hot design realizations are τ-equivalent.

References:

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