Classification of Sequential Circuits Based on Combinational Test Generation Complexity

Chia Yee Ooi † and Hideo Fujiwara †

† Graduate School of Information Science, Nara Institute of Science and Technology
8916-5 Takayama, Ikoma, Nara 630-0192, Japan

{chiaye-o, fujiwara}@is.aist-nara.ac.jp

Abstract

Several classes of sequential circuits with combinational test generation complexity have been introduced. However, no general notation is used to define the time complexity of test generation. In this paper, we introduce a new test generation notation that we call τ^k notation in order to present and clarify the classification of sequential circuits based on the combinational test generation complexity. For a class of sequential circuits, the time complexity of test generation is τ^k-bounded if it is $O(\tau^k(n))$ and τ^k-equivalent if it is $\Theta(\tau^k(n))$, where $\tau(n)$ is the combinational test generation complexity and n is the size of the circuits. Based on τ^k notation, we reconsider the time complexity of test generation for the existing classes of acyclic sequential circuits including balanced sequential circuits, strongly balanced sequential circuits, and internally balanced sequential circuits. In this paper, we also introduce a new method of design for testability called feedback shift register scan design (FSR scan design) technique, which is extended from the scan design technique. We discuss the time complexity of test generation for the scan designed circuits and the FSR scan designed circuits. We also introduce three classes of sequential circuits, which are τ-equivalent and τ^2-bounded. The k-length-bounded testable circuits is identified as a class of sequential circuits with τ^2-bounded time complexity if the parameter k is O(n) while k-time-bounded testable circuits and k-time-bounded validity-identifiable circuits are identified as classes with τ-equivalent (τ^2-bounded) time complexity if the parameter k is $\tau(n)$ ($\tau^2(n)$).

Keywords: *test generation complexity, τ^k notation, easily testable, design for testability*

1. Introduction

It has been known for more than two decades that the test generation problem is NP-complete. However, empirical observation shows that the combinational test generation complexity seems to be $O(n^r)$ for some constant r, where n is the size of the circuit. From this point of view, works have been done on searching for classes of sequential circuits with test generation problem that can be reduced to the combinational test generation problem, or simply, classes of sequential circuits with combinational test generation complexity.

Balanced sequential circuits [1] is one of the classes of circuits with combinational test generation complexity. In [2], its subclass that consists of strongly balanced sequential circuits is introduced. For each sequential circuit of these classes [1, 2], combinational ATPG can be used to generate the test patterns by treating the circuit as being combinational, with all registers in the circuit replaced by delayless wires. A specialized test generation model (TGM) in [3] shows that the test generation problem for acyclic sequential circuits can be reduced to a combinational test generation problem with multiple faults and logic duplicates. Internally balanced sequential circuits [4] is then identified as a larger class of sequential circuits that has combinational test generation complexity. This means a sequential circuit is internally balanced if it is balanced but the converse is not always true. Register-transfer level (RTL) designs with combinational test generation complexity include switched balanced sequential circuits [5] and switched internally balanced sequential circuits [6].

At first glance, the previous works mentioned above [1, 2, 3, 4, 5, 6] seem to have reduced the test generation problem to that with combinational test generation complexity. However, from the aspect of complexity analysis, acyclic sequential circuits presented in [3] does not allow combinational test generation complexity. In [3], TGM transforms an acyclic sequential circuit into its combinational equivalent with logic duplicates. The size of the combinational equivalent becomes larger and subsequently the time complexity for the test generation becomes greater as well. On the other hand, the test generation problem for general sequential circuits, which is modeled by an iterative logic array, possesses greater time complexity than that of acyclic sequential circuits does. To clarify the time complexity of test generation, we introduce a new concept for classification of sequential circuits based on combinational test generation complexity. In our discussion, we make an assumption that combinational test generation problem is solvable in polynomial time, which has been shown in the empirical observation mentioned above.

In Section 2, based on the asymptotic notation, we define the new test generation notation that we call τ^k notation. In section 3, we reconsider the time complexity of test generation for the existing classes of acyclic sequential circuits. A new technique of design for testability called FSR scan design is proposed in the next section. The time complexity of test generation for the scan designed circuits and the FSR scan designed circuits are also discussed. In Section 5, several τ-equivalent and τ^2-bounded classes of sequential circuits, which include some cyclic sequential circuits, are introduced. Conclusion is presented in the final section.

2. Preliminaries

Testing problem has been researched for many years. Several test generation algorithms have been introduced. Some of the popular test generation algorithms for combinational circuits are D-Algorithm [7], PODEM [8], FAN [9], TOPS [10], SOCRATES [11], SPIRIT [12] and so on. To facilitate our discussion, we define the time complexity of test generation problem as follows.

P_C: **Combinational Test Generation Problem**
Instance: A combinational circuit C and a fault f.
Question: Is there a test pattern to detect f in C?
P_S: **Sequential Test Generation Problem**

Instance: A sequential circuit S and a fault f.
Question: Is there a test sequence to detect f in S?
P_α: **Class α Test Generation Problem**
Instance: A sequential circuit S in α and a fault f.
Question: Is there a test sequence to detect f in S?

Definition 1: *The time complexity of a problem P* is the time complexity of the fastest algorithm for the problem P. Let $T_C(n)$, $T_S(n)$ and $T_\alpha(n)$ be the time complexity of P_C, P_S and P_α, respectively, where n is the size of the problem instance. $T_C(n)$, $T_S(n)$ and $T_\alpha(n)$ are also called *test generation complexity* for class *C*, class *S* and class α, respectively.

Generally, asymptotic notation is used to describe the asymptotic running time of an algorithm. This notation is also convenient for describing the worst-case running time of the test generation problem. The following describes briefly the notation. For a given function g(n), the set of functions can be denoted by Θ(g (n)) or Θ-notation as follows.

$\Theta(g(n))$ = {f(n): there exist positive constants c_1, c_2 and n_0 such that $0 \le c_1 g(n) \le f(n) \le c_2 g(n)$ for all $n \ge n_0$}.

A function f(n) belongs to the set Θ(g(n)) if there exist positive constants c_1 and c_2 such that it can be inserted between $c_1 g(n)$ and $c_2 g(n)$, for sufficiently large n. In other words, g(n) is an asymptotically tight bound for f(n). The Θ-notation asymptotically bounds a function from above and below. When there is only an asymptotic upper bound, the O-notation is used. For a given function g(n), the set of functions can be denoted by O(g(n)) as follows.

$O(g(n))$ = {f(n): there exist positive constants c and n_0 such that $0 \le f(n) \le cg(n)$ for all $n \ge n_0$}.

The O-notation gives an upper bound on a function to within a constant factor while Ω–notation provides an asymptotic lower bound. For a given function g(n), we denote by Ω(g(n)) the set of functions

$\Omega(g(n))$ = {f(n): there exist positive constants c and n_0 such that $0 \le cg(n) \le f(n)$ for all $n \ge n_0$}.

Generally, P_C is NP-complete. Since empirical observation shows that $T_C(n)$ seems to be $O(n^r)$ for some constant r, where n is the size of the circuits, several works have been done to identify classes of sequential circuits with combinational test generation complexity. To further clarify the test generation complexity, we define τ^k notation based on asymptotic notation. To show that $T_C(n)$ is the basics of the time complexity of test generation problem, the notation of τ(n) is used to denote $T_C(n)$ in the following text, where $\tau(n) = \Theta(n^r)$ for some constant $r \ge 2$.

Definition 2: T(n) is *τ^k-equivalent* if $T(n)=\Theta(\tau^k(n))$ and *τ^k-bounded* if $T(n)=O(\tau^k(n))$, where k>0.

Definition 3: Class α is τ^k-equivalent if $T_\alpha(n) = \Theta(\tau^k(n))$ and τ^k-bounded if $T_\alpha(n) = O(\tau^k(n))$, where k>0.

The following section reconsiders the test generation complexity of the existing classes of acyclic sequential circuits based on τ^k notation.

3. Existing Classes of Acyclic Sequential Circuits

The test generation problem for the existing acyclic circuits in terms of τ^k notation give a clearer picture of the test generation complexity.

3.1 Balanced Sequential Circuits

Let a directed graph G=(V, A, H) represents a sequential circuit. V represents a set of clouds where each cloud is a maximal region of connected combinational logic such that its inputs are either primary inputs or outputs of registers and its outputs are either primary outputs or inputs to registers. A represents a set of connections between two clouds through a register. Arcs in $H \subset A$ represent HOLD registers. A sequential circuit is said to be a *balanced sequential circuit* if

1. G is acyclic;
2. $\forall v_i, v_j \in V$, all directed paths (if any) from v_i to v_j are of equal length;
3. $\forall h \in H$, if h is removed from G, the resulting graph is disconnected.

Theorem 1: Balanced sequential circuits is τ-equivalent.

Proof: [1] shows that every balanced sequential circuit can be transformed to its combinational equivalent by only replacing all registers in the circuit with delayless wires. The circuit transformation can be done in time O(n). Let $T_B(n)$ denotes the test generation complexity for balanced sequential circuits, where n is the size of the circuits. $T_B(n)$ consists of the circuit transformation time complexity and the test generation complexity for the combinational equivalent.

$$T_B(n) = O(n) + \tau(n)$$
$$= \Theta(\tau(n)).$$

From definition 2, balanced sequential circuits is τ-equivalent.

3.2. Strongly Balanced Sequential Circuits

Let a directed graph G=(V, A, w) represents a sequential circuit. V represents a set of clouds, where each cloud is a maximal region of connected combinational logic such that its inputs are either primary inputs or outputs of registers and its outputs are either primary outputs or inputs to registers. A represents a set of connections between two clouds. A weight, w(a) on the arc $a= (v_i , v_j)$ equals to the number of registers between the corresponding clouds. A sequential circuit is a *strongly balanced sequential circuit* when the following conditions are satisfied.

1. G is acyclic;
2. $\forall v_i, v_j \in V$, all directed paths (if any) from v_i to v_j are of equal length;
3. $t(v_i) = t(v_j)+w(a)$ $\forall a=(v_i , v_j)$, $t(v_i)$ and $t(v_j)$ are integer values assigned to v_i and v_j respectively.

Theorem 2: Strongly balanced sequential circuits is τ-equivalent.

Proof: Since strongly balanced sequential circuits is a subclass of balanced sequential circuits, a given strongly balanced sequential circuit can be transformed to its combinational equivalent by replacing all registers in the circuit with delayless wires. This can be done in time O(n). There is no logic duplication in the transformed circuit. Let $T_{SB}(n)$ denotes the test generation complexity for strongly balanced

sequential circuits, where n is the size of the circuits**.** $T_{SB}(n)$ consists of circuit transformation time complexity and the test generation complexity for the combinational equivalent of the sequential circuits.

$$T_{SB}(n) = O(n) + \tau(n) = \Theta(\tau(n)).$$

Therefore, strongly balanced sequential circuits is τ-equivalent.

3.3. Internally Balanced Sequential Circuits

According to [4], if a circuit resulting from operation 1 of the extended combinational transformation (C*-transformation) on an acyclic sequential circuit is a balanced sequential circuit, then the circuit is regarded as an *internally balanced sequential circuit*. C*-transformation consists of the following two operations.

1. For a primary input with fanout branches, the set of fanout branches of that primary input is denoted by X. Let us obtain the smallest partition of X which satisfies the following statement: If branches x_i and x_j belong to different blocks X(i), X(j) of partition $\prod$ ($x_i \subset X(i)$, $x_j \subset X(j)$, $X(i) \neq X(j)$), then x_i and x_j are separable. Each partitioned block is provided with a new primary input separated from the original primary input;
2. All flip-flops are replaced by wires.

Theorem 3: Internally balanced sequential circuits is τ-equivalent.

Proof: [4] has proved that if a fault f in an internally balanced sequential circuit, S can be tested then the corresponding fault f_C in C*(S) can be tested. And, there is no logic duplication in C*-transformation. C*(S) can be done in time $O(n^2)$. Let $T_{IB}(n)$ denotes the test generation complexity for internally balanced sequential circuits, where n is the size of the circuits. $T_{IB}(n)$ includes C*-transformation time complexity and the test generation complexity for the combinational equivalent. Then, the test generation time complexity is

$$T_{IB}(n) = O(n^2) + \tau(n) = \Theta(\tau(n)).$$

From definition 2, internally balanced sequential circuits is τ-equivalent.

3.4. Acyclic Sequential Circuits

An *acyclic sequential circuit* is a sequential circuit without feedback. Based on the technique in [3], the test generation for acyclic sequential circuits invokes logic duplication. Thus, the test generation complexity for acyclic sequential circuits is τ^2-bounded. Let $T_A(n)$ be the test generation complexity for acyclic sequential circuits. "Is $T_A(n)$ τ-equivalent?" is still an open question. No one has proved the answer is "Yes" but it might probably be "No" since the existing works show that generally in the time expansion model for the test generation problem, the logic duplication might happen for at most d time frames, where d is the sequential depth. So, we have the following conjecture.

Conjecture 1: Acyclic sequential circuits is not τ-equivalent.

Although the test generation complexity of acyclic sequential circuits may not be τ-equivalent, the practical observation shows that its time complexity is close to $\Theta(\tau(n))$ instead of $\Theta(\tau^2(n))$. This means the test generation for acyclic sequential circuits is still not very hard. Thus, we introduce the following theorem.

Theorem 4: Acyclic sequential circuits is τ^2-bounded.

Proof: [3] shows that the number of time frames in which logic duplication might take place is at most d, where d is the sequential depth. In other words, the time complexity for the logic duplication is $O(n \bullet (d+1))$. Let $T_A(n)$ denotes the test generation complexity for acyclic sequential circuits, where n is the size of the circuits. $T_A(n)$ consists of the circuit transformation time complexity and the test generation complexity for the combinational equivalent. Thus, the test generation complexity becomes as follows.

$T_A(n) = O(n \bullet (d+1)) + \tau(n \bullet (d+1))$
$T_A(n) = O(\tau^2(n))$ for $d \leq n$.

From definition 2, $T_A(n)$ is τ^2-bounded.

Figure 1 illustrates the relationship between these classes of acyclic sequential circuits.

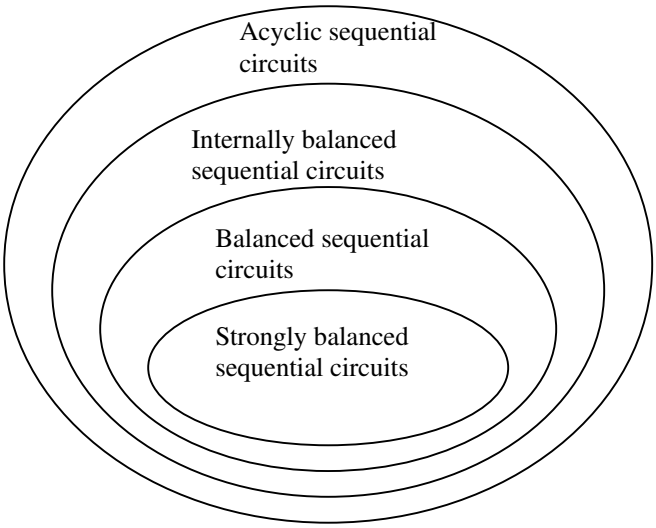

Figure 1. Classes of acyclic sequential circuits

4. Scan Designed Circuits and FSR Scan Designed Circuits

Test generation for sequential circuits is, in general, a difficult and intractable task, which may be unsolvable within a reasonable time for a large-scale circuit. Design for testability like scan design technique is one of the solutions to reduce the test generation complexity. Scan designed circuits are sequential circuits that are augmented by scan design technique. In the scan design technique, some or all of the flip-flops are replaced by scan flip-flops and thus can be directly controlled and observed. This technique is very well known since it can reduce the test generation complexity. In this section, we propose a new method of design for testability called FSR scan design technique, which is extended from the scan design technique. Sequential circuits that are augmented by this technique are called FSR scan designed circuits. This section also discusses the test generation complexity for the scan designed circuits and the FSR scan designed circuits in a new perspective.

4.1. Scan Designed Circuits

A sequential circuit is a *scan designed circuit* (Figure 3) if some or all of the flip-flops are replaced with *scan flip-flops* (Figure 2) so that they are chained into a shift register during test mode and hence they can be directly controlled and observed. When all the flip-flops of a circuit are replaced with scan flip-flops, this circuit is called full scan designed circuit, and the remaining circuit (the kernel) is a combinational circuit. When only some flip-flops of a circuit are replaced with scan flip-flops, the circuit is called partial scan designed circuit, and the kernel is a sequential circuit.

Theorem 5: The test generation complexity for the scan designed circuits is τ^k-equivalent (τ^k-bounded) if the test generation complexity for the kernels is τ^k-equivalent (τ^k-bounded).

Proof: The scan flip-flops are treated as equivalents to external I/O terminals and the test generation is performed for the kernel. The test patterns required by the scan flip-flops can be shifted into the scan chains during test application. Hence, the test generation complexity for a scan designed circuit is the test generation complexity for the kernel of the circuit.

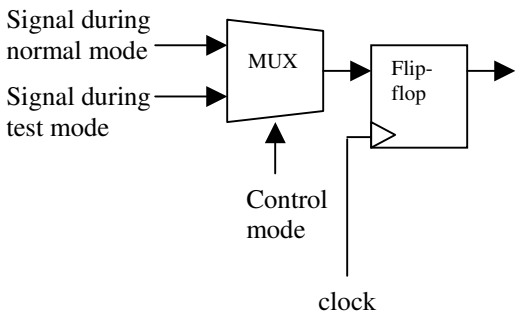

Figure 2. Scan flip-flop

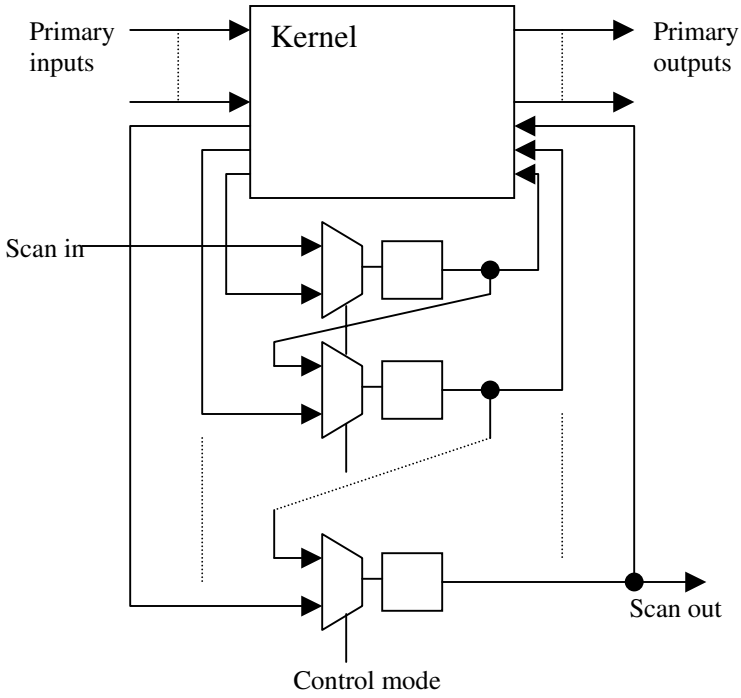

Figure 3. Scan designed circuit

4.2. FSR Scan Designed Circuits

A sequential circuit is an *FSR scan designed circuit* (Figure 5) if some or all of the shift registers are converted into *scan shift registers* (Figure 4) so that the scan shift registers are chained together during test mode and hence they can be directly controlled and observed. Each shift register has its own length *l*. The remaining circuit (called the kernel) is a combinational circuit when all the flip-flops are converted into scan shift registers. Otherwise, the kernel is a sequential circuit. We call this design technique as FSR scan design technique.

Theorem 6: The test generation complexity for the FSR scan designed circuits is τ^k-equivalent (τ^k-bounded) if the test generation complexity for the kernels is τ^k-equivalent (τ^k-bounded).

Proof: The scan shift registers are treated as equivalents to external I/O terminals and the test generation is performed for the kernel. The test patterns required by the scan shift registers can be shifted in during test application. Hence, the test generation complexity for FSR scan designed circuits is the test generation complexity for the kernels of the circuits.

Not all sequential circuits can be augmented to the FSR scan designed circuit except the trivial augmentation of using only scan shift registers of length 1. Note that the scan design is a special case of the FSR scan design. FSR scan design technique is always an attractive approach to the design for testability. This is because it requires little extra circuit for scan and thus it is expected to have less area overhead.

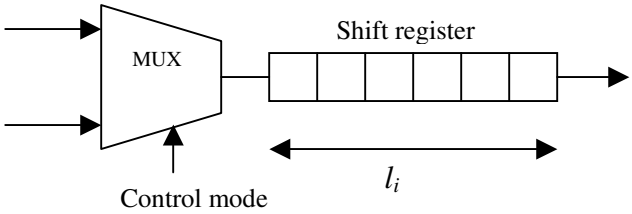

Figure 4. Scan shift register.

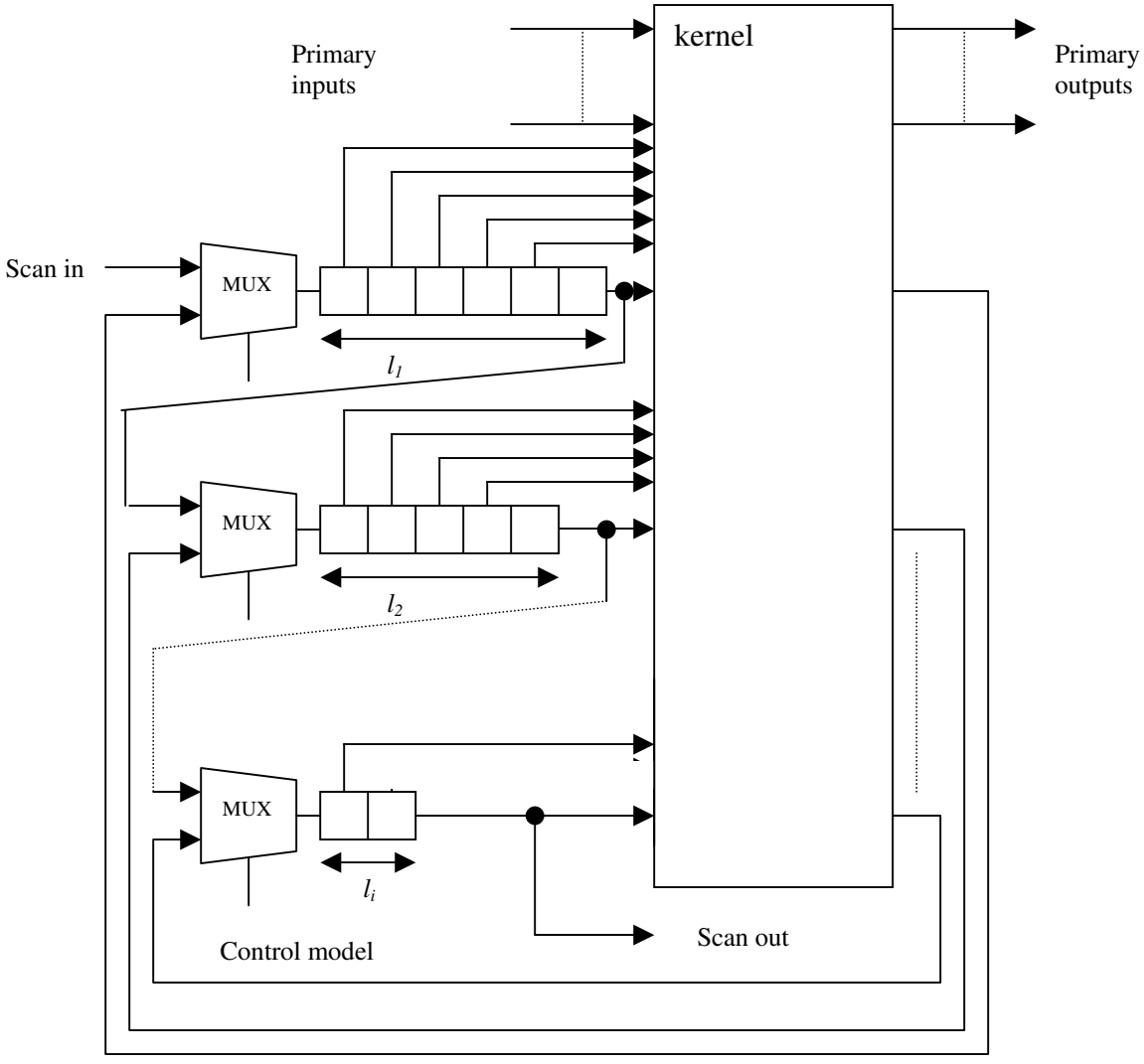

Figure 5. FSR scan designed circuit.

5. Classes of Easily Testable Sequential Circuits

In this paper, we consider a class is *easily testable* if its test generation complexity is τ^2-bounded. In other words, τ^2-bounded classes and τ-equivalent classes are easily testable. As mentioned in the previous section, when design for testability augments an arbitrary sequential circuit to a circuit with easily testable kernel, the test generation complexity of the circuit becomes easily testable as well. When fewer flip-flops or shift registers are scanned, the area overhead of the augmented circuits is reduced. Since a larger class means fewer flip-flops or shift registers need to be scanned in order to ensure the kernels is single-pattern testable, it is important to identify larger classes of kernels that are easily testable. In previous works, acyclic sequential circuits have been identified to be easily testable. In this section, we introduce three classes of easily testable sequential circuits, which include some cyclic sequential circuits. These classes have less area overhead and at the same time, have similar test generation complexity compared to the acyclic sequential circuits.

Generally, the test generation problem for a cyclic sequential circuit is modeled by an iterative logic array that consists of several time frames (Figure 6) so that it can be solved by combinational test generation techniques. The test generation problem involves the following three steps.

1. Derivation of the excitation state for a fault in the combinational part by treating the present-state (PS) lines as primary inputs and the next-state (NS) lines as primary outputs. This step is performed on the combinational part at time frame 0. The excitation state propagates the fault effect to the primary outputs or next-state lines;
2. State justification, which considers the fault effect in all time frames. This step extends the iterative array in backward direction for *i* time frames, where *i* is a positive integer;
3. State differentiation, which considers the fault effect in all time frames. This step extends the iterative array in forward direction for *j* time frames, where *j* is a positive integer.

State differentiation that considers the fault effect in all time frames is also called fault propagation. Generally, backtrack might occur between the three steps. For a given fault, step 1 is performed to obtain an excitation state for state justification and fault propagation. If state justification or fault propagation fails, step 1 is performed again to get a different excitation state for justification and fault propagation. Logic duplication of the circuit combinational part takes place at every time frame except time frame 0. The number of time frames affects significantly the test generation complexity. In the worst case, *i* and *j* are at most 2^p, where p is the number of memory elements or state variables. This is impractical because the test generation complexity is exponential. Note that the state justification that fail to justify an excitation state and the fault propagation that fail to propagate the fault effect to any primary output are also taken into account in determining the time complexity of the state justification T_J and the time complexity of the fault propagation T_D respectively.

However, there are exceptional classes of sequential circuits with τ-equivalent or τ^2-bounded test generation complexity, which include some cyclic sequential circuits. In such classes, backtrack between the state justification, fault propagation and derivation of excitation state do not occur. Since the derivation of the excitation state is done by test generation on the combinational part at time frame 0, the time complexity $T_E(n)$ is always τ-equivalent. Therefore, the testability of cyclic sequential circuits depends on the time complexity for the state justification and fault propagation. If the state justification and fault propagation can be reduced to problem with τ^2-bounded or τ-equivalent or less time complexity, the circuits become easily testable. The test generation complexity for a class of easily testable sequential circuits, $T_S(n)$ is

$$T_S(n) \leq T_E(n) + T_J + T_D$$
$$= \tau(n) + T_J + T_D \text{, where } T_J, T_D = O(\tau(n)) \text{ or } O(\tau^2(n)).$$

The following sub-sections introduce three classes of easily testable sequential circuits with τ^2-bounded or τ-equivalent test generation complexity, which cover some cyclic sequential circuits.

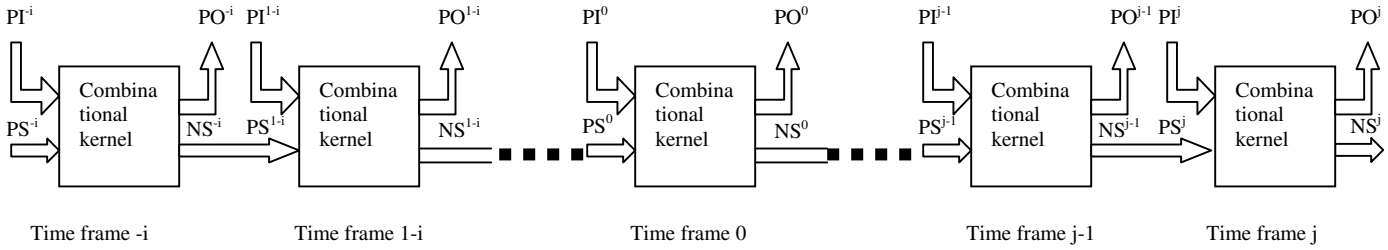

Figure 6. Iterative logic array model.

5.1. Length-Bounded Testable Circuits

As mentioned above, the testability of the cyclic sequential circuits depends on the time complexity of state justification and fault propagation. The number of time frames expanded by the justification and fault propagation accounts for the length of a test sequence. In this section, we introduce a class of sequential circuits called length-bounded testable circuits, the test sequence length of which can be bounded so that the class becomes easily testable. A length-bounded testable circuit is defined as follows.

Definition 4: A sequential circuit *S* is *k-length-bounded testable* with respect to a fault set *F* if the following conditions are satisfied.

1. For any state s_i , there exists a state justification sequence of length at most k;
2. For any pair of states (s_i, s_{if}), there exists a fault propagation sequence of length at most k, where s_i is a fault-free state and s_{if} is a faulty state corresponding to a fault *f* and $f \in F$.

Theorem 7: k-length-bounded testable circuits is τ^2-bounded if k is O(n), where n is the size of the sequential circuits.

Proof: To generate a test sequence for a given fault *f* in a k-length-bounded testable circuit, firstly combinational test generation is performed at time frame 0 to derive an excitation state so that *f* is excited and propagated to next-state lines or primary outputs. Secondly, state justification sequence is generated for the excitation state s_i and lastly if the fault effect is not propagated to primary output by the first two steps, fault propagation sequence is generated for a pair of (s_i, s_{if}), where s_{if} is the next state of time frame 0 and s_i is the corresponding state in the fault-free circuit. Condition 1 of definition 4 guarantees that for any state s_i, there exists a state justification sequence and condition 2 of definition 4 guarantees that for any pair of states (s_i, s_{if}), there exists a fault propagation sequence. Consequently, the test sequence generation for a given fault is a one-way procedure consisting of the three steps mentioned above, which means no backtracks occur between the steps. Condition 1 of definition 4 implies that the state justification expands the combinational part for at most k time frames to justify the excitation state s_i. Therefore, the justification is performed on the combinational part duplication of size at most k•n. Generally, the time complexity of the state justification T_J for an excitation state is τ–bounded ($T_J(n)=O(\tau(n))$). The time complexity of the state justification $T_J(k \bullet n)$ is

$$T_J(k \bullet n) = O(\tau(k \bullet n)).$$

Condition 2 of definition 4 implies that the fault propagation expands the combinational part for at most k time frames in order to propagate the fault effect from time frame 0 to primary output.

Therefore, the fault propagation is performed on the combinational part duplications of size at most k•n. Generally, the time complexity of the fault propagation T_D for an activated fault is τ–bounded ($T_D(n)=O(\tau(n))$). The time complexity of the fault propagation $T_D(k\bullet n)$ is

$T_D(k\bullet n) = O(\tau(k\bullet n))$.

Let $T_{LBT}(n)$ be the test generation complexity for k-length-bounded testable circuits and k be O(n). Then, we have

$$\begin{aligned} T_{LBT}(n) &\le T_E(n)+T_J(k\bullet n)+ T_D(k\bullet n) \\ &= \tau(n) + O(\tau(k\bullet n)) + O(\tau(k\bullet n)) \\ &= \tau(n) + O(\tau^2(n)) + O(\tau^2(n)) \text{ for k is O(n)} \\ &= O(\tau^2(n)). \end{aligned}$$

Hence, the test generation complexity for the k-length-bounded testable circuits is τ^2-bounded if k is O(n).

5.2. Time-Bounded Testable Circuits

In this section, a class of sequential circuits called time-bounded testable circuits is introduced. Instead of being bounded by the test sequence length, the state justification and fault propagation for this class is bounded by the time complexity, which is a stronger condition. The time-bounded testable circuit is defined as follows.

Definition 5: A sequential circuit *S* is *k-time-bounded testable* with respect to a fault set *F* if the following conditions are satisfied.

1. For any state s_i, there exists a state justification sequence which can be obtained in time O(k);
2. For any pair of states (s_i, s_{if}), there exists a fault propagation sequence which can be obtain in time O(k), where s_i is a fault-free state and s_{if} is a faulty state corresponding to a fault *f* and $f \in F$.

Theorem 8: k-time-bounded testable circuits is τ-equivalent (τ^2-bounded) if k is $\tau(n)$ ($\tau^2(n)$), where n is the size of the sequential circuits.

Proof: To generate a test sequence for a given fault *f* in a k-time-bounded testable circuit, firstly combinational test generation is performed at time frame 0 to derive an excitation state so that *f* is excited and propagated to next-state lines or primary outputs. Secondly, state justification sequence is generated for the excitation state s_i and lastly if the fault effect is not propagated to primary output by the first two steps, fault propagation sequence is generated for the pair of states (s_i, s_{if}), where s_{if} is the next state of time frame 0 and s_i is the corresponding state in fault-free circuit. Condition 1 of definition 5 guarantees that for any state s_i, there exists a state justification sequence and condition 2 of definition 5 guarantees that for any pair of states (s_i, s_{if}), there exists a fault propagation sequence. Consequently, the test sequence generation for a given fault is a one-way procedure consisting of the above three steps, which means no backtracks occur between the steps. From condition 1 of definition 5, we have

$T_J = O(k)$.

From condition 2 of definition 5, we have

$T_D = O(k)$.

Let $T_{TBT}(n)$ be the test generation complexity for k-time-bounded testable circuits. Then,

$$\begin{aligned} T_{TBT}(n) &\le T_E(n)+ T_J+ T_D \\ &= \tau(n)+ O(k)+ O(k) \\ &= \tau(n)+ O(\tau(n))+ O(\tau(n)) \text{ for k be } \tau(n) \\ &= \Theta(\tau(n)). \end{aligned}$$

Hence, the test generation complexity for k-time-bounded testable circuits is τ-equivalent if k is $\tau(n)$.

In the case where k is $\tau^2(n)$, we have

$$\begin{aligned} T_{TBT}(n) &\le T_E(n)+ T_J+ T_D \\ &= \tau(n) + O(k) + O(k) \\ &= \tau(n) + O(\tau^2(n))+ O(\tau^2(n)) \text{ for k be } \tau^2(n) \\ &= O(\tau^2(n)). \end{aligned}$$

Therefore, k-time-bounded testable circuits is τ^2-bounded if k is $\tau^2(n)$.

Example: State-shiftable FSM realization.

A *state-shiftable FSM* [14] is an easily testable machine that possesses

1. transfer sequences of length at most $[\log_2 m]$ to carry the machine from state s_0 to state s_i for all i, where m denotes the number of states, and
2. distinguishing sequences of length $[\log_2 m]$, which are arbitrary input sequence consisting of 2 input symbols, ε_0 and ε_1.

A sequential circuit that is realized from the machine is called state-shiftable FSM realization. State-shiftable FSM realization belongs to the k-time-bounded testable circuits with k be $\tau(n)$ under the assumption that the sub-circuit with output function $\delta(s_i, \varepsilon_0)$ and $\delta(s_i, \varepsilon_1)$ are fault-free, where s_i is any state. After deriving the excitation state s_i for a given fault in a state-shiftable FSM realization, a state can be justified by simulating the circuit with an input sequence consisting of 2 input symbols ε_0 and ε_1 for at most $[\log_2 m]$ transitions, where m is the number of states. Therefore, the time complexity of state justification is always τ-bounded.

$$\begin{aligned} T_J(n \bullet \log_2 m) &= O(n \bullet \log m) \\ &= O(n^2) \text{ for } \log m = O(n). \end{aligned}$$

Let s_{if} be the state of the circuit after the fault effect is propagated to next-state lines at time frame 0 and s_i be the corresponding state in the fault-free circuit. s_i and s_{if} can be differentiated by simulating the circuit with any input sequence consisting of 2 input symbols ε_0 and ε_1 for at most $[\log_2 m]$ transitions. In other words, a fault effect can be propagated to a primary output by simulating the circuit with any input sequence consisting of 2 input symbols ε_0 and ε_1 for at most $[\log_2 m]$ transitions. The time complexity of the fault propagation is also τ-bounded.

$$\begin{aligned} T_D(n \bullet \log_2 m) &= O(n \bullet \log m) \\ &= O(n^2) \text{ for } \log m = O(n). \end{aligned}$$

Let $T_{SS}(n)$ be the test generation complexity of the state-shiftable FSM realization.

$T_{SS}(n) \leq T_E(n) + T_J(n \bullet \log_2 m) + T_D(n \bullet \log_2 m)$
$= \tau(n) + O(n^2) + O(n^2)$
$= \Theta(\tau(n))$.

Therefore, from definition 2, the state-shiftable FSM realization is τ-equivalent.

5.3. Time-Bounded Validity-Identifiable Circuits

The test generation of the time-bounded validity-identifiable circuits is also bounded by the time complexity. Different from the time-bounded testable circuits, the circuits has easily identifiable valid states and the state validity information, i.e. density of encoding is taken into account in the test generation. Density of encoding is defined as the fraction of the total number of possible states, which are valid [13].

$$\text{Density of encoding} = \frac{number\ \ of\ \ valid\ \ states}{number\ \ of\ \ all\ \ states}$$

A time-bounded validity-identifiable circuit is defined as follows.

Definition 6: A sequential circuit *S* is *k-time-bounded validity-identifiable* with respect to a fault set *F* if the following conditions are satisfied.

1. There exists a combinational circuit of size O(n) called validity checker that can identify the validity of states, where n is the size of the sequential circuits;
2. For any valid state s_i, there exists a state justification sequence which can be obtained in time O(k);
3. For any pair of states (s_i, s_{if}), there exists a fault propagation sequence which can be obtained in time O(k), where s_i is a fault-free valid state and s_{if} is a faulty state corresponding to a fault *f* and $f \in F$.

Theorem 9: k-time-bounded validity-identifiable circuits is τ-equivalent (τ^2-bounded) if k is τ(n) ($\tau^2(n)$), where n is the size of the sequential circuits.

Proof: From condition 1 of definition 6, prior to the test sequence generation of a time-bounded validity-identifiable circuit a combinational circuit of size O(n) that can identify the validity of the states is constructed and embedded in the combinational part C of the time-bounded validity-identifiable circuit such that any excitation state s_i derived by the combinational test generation is a valid state. The transformed combinational part as shown in figure 7 is denoted by C', which has size O(2•n). It can be shown that a fault is testable in C with a valid state if and only if the fault is testable in C'. To generate a test sequence for a given fault *f* in a time-bounded validity-identifiable circuit, firstly combinational test generation is performed on C' at time frame 0 to derive an excitation state s_i so that *f* is excited and propagated to next-state lines or primary outputs. Note that s_i is a valid state. Secondly, state justification sequence is generated for the excitation state s_i and lastly if the fault effect is not propagated to primary output by the first two steps, fault propagation sequence is generated for a pair of states (s_i, s_{if}), where s_{if} is the next state of time frame 0 and s_i is the corresponding state in fault-free circuit. Condition 2 guarantees that for any valid state s_i, there exists a state justification sequence and condition 3 guarantees that for any pair of states (s_i, s_{if}), there exists a fault propagation sequence. Consequently, the test sequence generation is a one-way procedure consisting of the above three steps,

which means no backtracks occur between the steps. Let $T_E(2 \bullet n)$ be the test generation complexity of C'. The derivation of excitation state can be done in

$$\begin{aligned} T_E(2 \bullet n) &= \tau(2 \bullet n) \\ &= \tau(n). \end{aligned}$$

From condition 2 of definition 6, we have

$$T_J = O(k).$$

From condition 3 of definition 6, we have

$$T_D = O(k).$$

Let $T_{TBVI}(n)$ be the test generation complexity for time-bounded validity-identifiable circuits. Then,

$$\begin{aligned} T_{TBVI}(n) &\leq T_E(n) + T_J + T_D \\ &= \tau(n) + O(k) + O(k) \\ &= \tau(n) + O(\tau(n)) + O(\tau(n)) \text{ for k is } \tau(n) \\ &= \Theta(\tau(n)). \end{aligned}$$

Hence, time-bounded validity-identifiable circuits is τ-equivalent if k is $\tau(n)$.

If k be $\tau^2(n)$, then we have

$$\begin{aligned} T_{TBVI}(n) &\leq T_E(n) + T_J + T_D \\ &= \tau(n) + O(k) + O(k) \\ &= \tau(n)) + O(\tau^2(n)) + O(\tau^2(n)) \text{ for k is } \tau^2(n) \\ &= O(\tau^2(n)). \end{aligned}$$

Therefore, the time-bounded validity-identifiable circuits is τ^2-bounded if k is $\tau^2(n)$. Based on the above proof, we conclude that time-bounded validity-identifiable circuits is a class of easily testable sequential circuits.

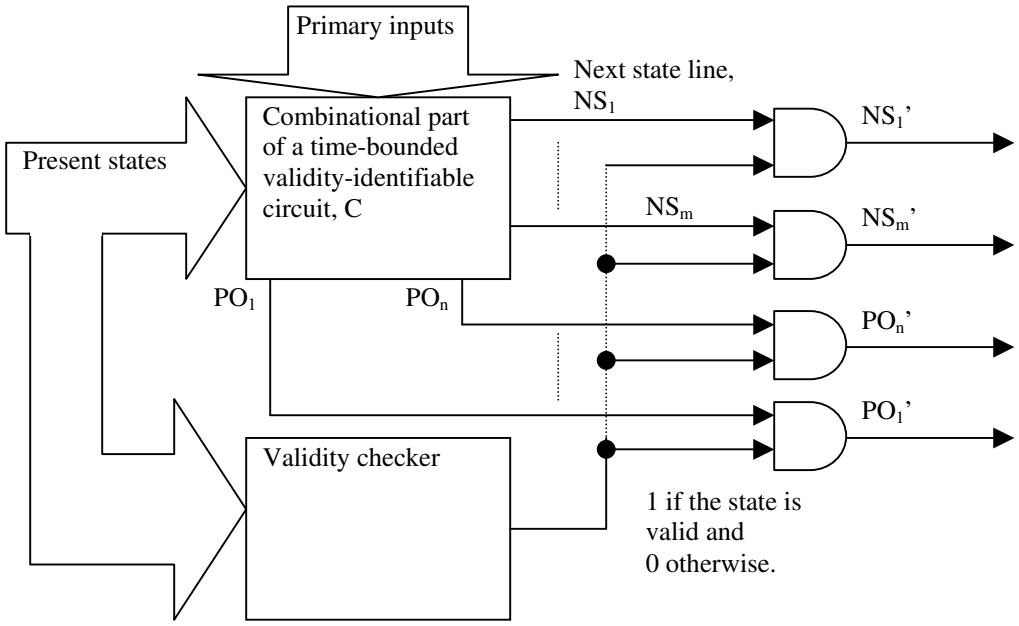

Figure 7. Transformed combinational part C' of a time-bounded validity-identifiable circuit.

Example: Counter-cycle validity-identifiable circuit.

A counter-cycle validity-identifiable circuit satisfies the following conditions:

1. Valid states are encoded by error-detecting code (EDC), where the number of valid states is in O(n) and there exists a validity checker of size O(n).
2. There exists an input symbol ε that strongly connects all the EDC-encoded valid states in S_V in a counter cycle and distinguishes between initial state s_0, other valid states (in S_V-{s_0}) and invalid states in S_{IV} such that
    a. the output function $\lambda(s_i, \varepsilon)=z_3$ if the state transition function $\delta(s_i, \varepsilon)=s_0$;
    b. the output function $\lambda(s_i, \varepsilon)=z_0$ if the state transition function $\delta(s_i, \varepsilon)\in S_V$-{$s_0$}; and
    c. the output function $\lambda(s_j, \varepsilon)=z_1$ or z_2 where s_i, $s_0\in S_V$, s_0 is also the initial state of the counter cycle, $s_j\in S_{IV}$ and $z_0, z_1, z_2, z_3\in Z=\{00, 01, 10, 11\}$;
3. Output logic and next-state logic are separate;
4. For any pair of state (s_i, s_k) where $s_i\in S_V$ and $s_k\in S= S_V\cup S_{IV}$, there exists an input symbol ε_{ik} such that $\lambda(s_i, \varepsilon_{ik})\neq\lambda(s_k, \varepsilon_{ik})$; and

Counter-cycle validity-identifiable circuit belongs to the k-time-bounded validity-identifiable circuits with k be $\tau(n)$ under the assumption that multiple-faults do not exist both in output logic and next-state logic. To generate a test sequence for a given fault *f*, a validity checker is constructed in time O(n) to transform the combinational part C into C'. Secondly, an excitation state s_i, which is guaranteed to be a valid state by its validity checker, is derived at time frame 0. Therefore,

$$T_E(2\bullet n) = \tau(2\bullet n) = \tau(n).$$

Then, a state justification sequence is obtained by simulating the circuit with input symbol ε for at most O(n) transitions in order to reach s_0 and for at most O(n) transitions in order to reach the excitation state s_i from s_0. Consequently,

$T_J(n^2) = O(n^2)$.

Lastly, fault propagation is performed with searching an input symbol ε_{ik} such that fault effect can be propagated to a primary output at time frame 1. The fault propagation requires time complexity

$T_D(n) = O(\tau(n))$.

Let $T_{CCVI}(n)$ be the test generation complexity for the counter-cycle validity-identifiable circuits. We have

$$\begin{aligned} T_{CCVI}(n) &\le T_E(n) + T_J + T_D \\ &= \tau(n) + O(n^2) + O(\tau(n)) \\ &= \Theta(\tau(n)). \end{aligned}$$

Therefore, counter-cycle validity-identifiable circuits is τ–equivalent.

6. Conclusion

τ^k notation has been introduced in order to clarify the test generation complexity. Based on this notation, the test generation complexity for balanced sequential circuits, strongly balanced sequential circuits, internally balanced sequential circuits have been proved as being τ-equivalent while the test generation complexity for acyclic circuits has been showed as being τ^2-bounded. We also introduced a new design for test method that is extended from the scan design method. The design for test method is called FSR scan design method. A sequential circuit that is augmented by the FSR scan design technique is called FSR scan designed circuit. The test generation complexity for the FSR scan designed circuits is shown to be equivalent to that of the circuit kernels. We introduced three classes of easily testable cyclic sequential circuits. The test generation complexity for the k-length-bounded testable circuits is τ^2-bounded if the parameter k is O(n) while the test generation complexity for k-time-bounded testable circuits and k-time-bounded validity-identifiable circuits is τ-equivalent (τ^2-bounded) if the parameter k is $\tau(n)$ ($\tau^2(n)$), where n is the size of the sequential circuits. Our future works are to find an effective design for test method and an efficient test generation algorithm for each easily testable class.

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