# Theorems for Separable Primary Input Faults in Internally Balanced Structures

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**Abstract** In our previous work, we introduced a new class of sequential circuits with combinational test generation complexity called *internally balanced* structure. We reduced the test generation problem for an internally balanced sequential circuit $S$ into the test generation problem for a combinational circuit $C$, where single stuck-at faults on all lines in $S$ except for some primary inputs, called *separable primary inputs*, correspond to single stuck-at faults on $C$. In this paper, we first show that test sequences for single stuck-at faults on fanout branches of separable primary inputs do not always detect faults on the primary inputs, and then present how to generate test sequences for single stuck-at faults on the separable primary inputs. As a result, the test generation problem for all single stuck-at faults in internally balanced circuits is reduced into the test generation problem for single stuck-at faults in combinational circuits.

## 1 Introduction

In [1], we introduced a new class of sequential circuits with combinational test generation complexity called *internally balanced* structure. We reduced the test generation problem for stuck-at faults in a circuit $S$ with internally balanced structure into the test generation problem for stuck-at faults in a combinational circuit $C$ where some primary input with fanout branches in $S$ are separated into two or more primary inputs according to some partition of the fanout branches. We call such primary inputs in $S$ *separable primary inputs*. Each single stuck-at fault on a separable primary input in $S$ corresponds to a multiple stuck-at fault on (all) the separated primary inputs in $C$, while the other single stuck-at faults in $S$ correspond to single stuck-at faults in $C$. Therefore, we needed a test pattern generation algorithm for multiple stuck-at faults to find test sequences for single stuck-at faults on separable primary inputs. We shall consider only stuck-at faults in this paper, and refer *stuck-at faults* to hereafter just as *faults*.

We first show that test sequences corresponding to test patterns for single faults on separated primary inputs do not always detect faults on the separable primary inputs. This means that even if we can find test patterns for all detectable faults on the separated primary inputs of a separable primary input $x$, test sequences corresponding to these test patterns may not detect the fault on $x$ though it is detectable.

We then present how to find test sequences for single faults on the separable primary inputs. We show that we can get a test sequence for a single stuck-at-$v$ fault on a separable primary input directly from a test pattern for a single stuck-at-$v$ fault on one of the separated primary inputs. We also show that a single stuck-at-$v$ fault on a separable primary input is redundant if all single stuck-at-$v$ faults on the separated primary inputs are redundant. In this way, we reduce the test generation problem for single faults in circuits with internally balanced structures into the test generation problem for single faults in combinational circuits.

The rest of this paper in organized as follows. In Section 2, the internally balanced structure and some notations are provided. We show that faults on the separable primary inputs may not be detected by test sequences for the separated primary inputs, and show how to generate complete test sequences and identify redundancy in Section 3. Section 4 concludes the paper.

## 2 Preliminaries

First, we briefly define the internally balanced structure[1]. For simplicity, we shall limit flip-flops (referred to hereafter as FFs) to DFFs. Another kind of FFs can be handled similarly.

The number of FFs included in a path is called the sequential depth of the path. The largest sequential depth over the paths from the primary

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inputs of a sequential circuit to a primary output is regarded as the sequential depth of the primary output. The largest sequential depth over the primary outputs is regarded as the sequential depth of the sequential circuit. Suppose $x$ is a primary input with fanout branches, and $y_i$ and $y_j$ are branches of $x$. If there is no primary output that can be reached from $y_i$ and $y_j$ over equal depth paths, then $y_i$ and $y_j$ are called *separable*.

**Extended Combinational Transformation:** A transformation based on the following two operations with a sequential circuit $S$ of acyclic structure is called the extended combinational transformation
($C^*$-*transformation*), and the resulting combinational circuit is denoted by $C^*(S)$.

(1) **Separation of primary inputs:** For each primary input $x$ with fanout branches, *separate* it as follows. Let $Y$ denote a set of the fanout branches of a primary input. Let us obtain the smallest partition $\Pi$ of $Y$ which satisfies the following statement: If branches $y_a$ and $y_b$ belong to different blocks $Y(i)$, $Y(j)$ of partition $\Pi$ ($y_a \in Y(i)$, $y_b \in Y(j)$, $Y(i) \neq Y(j)$) then $y_a$ and $y_b$ are separable. As shown in Fig.1, each partitioned block $Y(i)$ is provided with a new primary input $x_i$ separated from the original primary input $x$.

(2) $C$**-transformation:** Replace each FF by a wire (for the case of negative FF output, a NOT gate is added, see Fig.2).

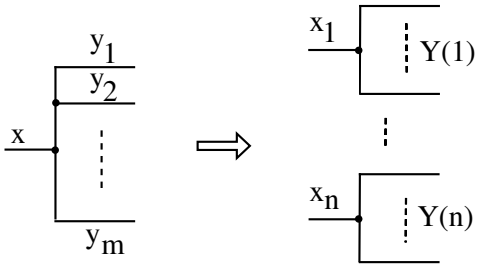



Figure 1: Primary input separation.

Note that we can uniquely obtain the smallest partition $\Pi$ for each primary input as connected components of a graph such that the vertices are the fanout branches and an edge exists iff two fanout branches are not separable. In this way, for a given acyclic circuit $S$, the resulting circuit from the operation (1) of the $C^*$-transformation and the resulting circuit from the $C^*$-transformation are uniquely determined. Let $S^*(S)$ and $C^*(S)$ denote these circuits, respectively.

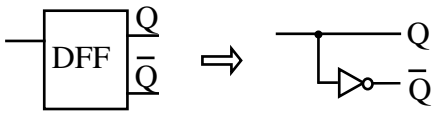



Figure 2: Deletion of flip-flops.

**Balanced Structure[2]:** For any pair of primary input and primary output in an acyclic circuit $S$, if the sequential depths of all paths connecting these two points are equal, then $S$ is regarded as a *balanced structure*.

**Internally Balanced Structure:** An acyclic circuit $S$ is regarded as an *internally balanced structure* if a circuit $S^*(S)$ is a balanced structure.

The circuit shown in Fig3 is an internally balanced structure but is not a balanced structure where $A, B, C, D$ are blocks of combinational logics and $R1$, $R2$, $R3$ are registers (collections of FFs). On the other hand, if the circuit is balanced structure then it is also internally balanced structure. The relation among the structures is as follows: {sequential circuits with acyclic structure} $\supset$ {sequential circuits with internally balanced structure}$\supset$ {sequential circuits with balanced structure}.

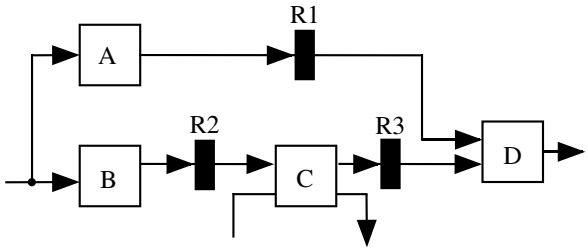



Figure 3: Example of internally balanced structure.

Let $S$ be a circuit with an internally balanced structure. We consider transformation of a test sequence $T$ for $S$ into a test pattern for $C^*(S)$. Let $z$ be a primary output in both $S$ and $C^*(S)$. We define transformation $T_c(T, S, z, \tau)$ of a test sequence $T$ for $S$ into a test pattern for $C^*(S)$ that determines the value of $z$ in time frame $\tau$ as

follows. Assume that the length of $T$ and $\tau$ is more than the sequential depth of $z$. In the following, if there is no path from a primary input $x$ to $z$ in $C^*(S)$, we consider the value of $x$ as *don't care*.

(1) Case where $x$ is not a primary input in $S$ separated in $C^*(S)$:
The sequential depth $d$ of any paths from $x$ to $z$ is uniquely determined. The value of $x$ in $T_c(T, S, z, \tau)$ is the value of $x$ of $T$ in time frame $\tau - d$.

(2) Case where $x$ is a primary input in $S$ separated in $C^*(S)$:
Assume that the primary input $x$ in $S$ is separated to obtain the primary inputs $x_1, x_2, \cdots, x_n$ in $C^*(S)$. Since $S$ is an internally balanced structure, any path from $x_j$ to $z$ has unique sequential depth $d_j$. The value of $x_j$ $(j = 1, 2, \cdots, n)$ of test pattern $T_c(T, S, z, \tau)$ is the value of $x$ of $T$ in time frames $\tau - d_j$ $(j = 1, 2, \cdots, n)$.

In the second case, since all sequential depths $d_j$ $(j = 1, 2, \cdots, n)$ are different and the values of $x_j$ $(j = 1, 2, \cdots, n)$ determine the values of $x$ of $T$ in different time frames. Therefore, we can define a test sequence $T$ from a test pattern $t$ satisfying $t = T_c(T, S, z, \tau)$.

In [1], we showed that the test generation problem for a sequential circuits $S$ with internally balanced structure can be reduced to the test generation problem for a combinational circuit $C^*(S)$. However, each fault on a separable primary input $x$ in $S$ corresponds to a multiple fault on all the separated primary inputs of $x$ in $C^*(S)$. On the other hand, any other single stuck-at-$v$ fault $f$ on a line $y$ (including the fanout branch) in $S$ corresponds to a single stuck-at-$v$ fault $f'$ on the same line $y$ in $C^*(S)$, and a test pattern $t$ detects $f'$ iff any test sequence satisfying $t = T_c(T, S, z, d)$ detects $f$ in $S$ where $t$ propagates a fault effect to a primary output $z$ with a sequential depth $d$.

# 3 Detection of Separable Primary Input Faults

In this section, we consider whether the test generation problem for *single* faults in sequential circuits with internally balanced structures can be reduced to the test generation problem for *single* faults in combinational circuits. We first consider the following conjecture.

**Conjecture 1** Let $S$ be a sequential circuit with internally balanced structure. The following statement holds for any primary input $x$ in $S$ which is separated into $x_1, x_i, \cdots, x_n$ in $C^*(S)$: If $\{t_1, t_2, \cdots, t_k\} \neq \emptyset$ is a complete test set for the single stuck-at-$v$ faults on $x_1, x_i, \cdots, x_n$ in $C^*(S)$ then there exists a test pattern $t \in \{t_1, t_2, \cdots, t_k\}$ such that any test sequences $T$ satisfying $t = T_c(T, S, z, d)$ detects a stuck-at-$v$ fault on $x$ in $S$ where $t$ propagates a fault effect to a primary output $z$ and $d$ is a sequential depth of $z$ in $S$.

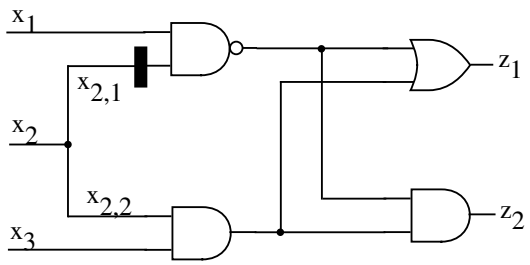
If the conjecture holds, we can generate a test sequence $T$ for a single stuck-at-$v$ fault on a separable primary input $x$ as follows: First generate test patterns for single stuck-at-$v$ faults on the separated primary inputs $x_1, x_2, \cdots, x_n$, then transform them to test sequences for $S$. One of the test sequences can detect a stuck-at-$v$ fault on $x$. In this way, we do not have to consider multiple faults in $C^*(S)$. However, the conjecture does not hold.

**Theorem 1** Conjecture 1 does not holds.

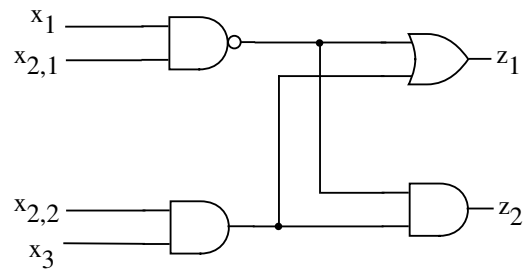
*Proof:* Consider the sequential circuit $S$ in Fig.4(a), where $S$ is an internally balanced structure and a primary input $x_2$ is separable. We can obtain a circuit $C^*(S)$ in Fig.4(b) where $x_2$ is separated into $x_{2,1}$ and $x_{2,2}$. To prove the theorem, it is sufficient to show that, for each $x_{2,j}$ $(j = 1, 2)$, there is a test pattern $t$ such that it detects a single stuck-at-$v$ fault on $x_{2,j}$ and some sequence $T$ satisfying $t = T_c(T, S, z, d)$ cannot detect a stuck-at-$v$ fault on $x_2$ where $t$ propagate a fault effect to a primary output $z$ and $d$ is the sequential depth of $z$ in $S$.

Now, we show such test patterns for stuck-at-1 faults on $x_{1,1}$ and $x_{2,1}$. Test pattern $t = (x_1 = 1, x_{2,1} = 0, x_{2,2} = 0, x_3 = 1)$ can detect both stuck-at-1 faults on $x_{1,1}$ and $x_{2,1}$ in $C^*(S)$. It propagates $D$ to $z_1$ for a fault on $x_{2,1}$ and $\bar{D}$ to $z_2$ for a fault on $x_{2,2}$. Both sequential depths of $z_1$ and $z_2$ are 1, and a sequence $T = 000, 101$ satisfies $t = T_c(T, S, z_1, 1)$ and $t = T_c(T, S, z_2, 1)$ but does not detect a stuck-at-1 fault on $x_2$. ■

Although Conjecture 1 does not hold, we can find a test sequence which detects a fault on a separable primary input. For an input pattern $t = (v_1, v_2, \cdots, v_m)$ for a combinational circuit with primary inputs $x_1, x_2, \cdots, x_m$, let $t[x_i := w_i, x_j := w_j, \cdots]$ denote the input pattern obtained from replacing the values of $x_i, x_j, \cdots$ with the values $w_i, w_j, \cdots$.




(a)




(b)

Figure 4: (a) Internally balanced structure $S$; (b) Combinational equivalent $C^*(S)$.

**Theorem 2** Let $S$ be a sequential circuit with internally balanced structure, where a primary input $x$ in $S$ is separated into $x_1, x_2, \cdots, x_n$ in $C^*(S)$. If $t$ is a test pattern for a single stuck-at-$v$ fault $f_j$ on some $x_j$ in $C^*(S)$, then a single stuck-at-$v$ fault $f$ on $x$ in $S$ can be detected by any $T$ satisfying $t = T_c(T, S, z, d)$ or any $T'$ satisfying $t[x_j := v] = T_c(T', S, z, d)$ where $z$ is the primary output to which $t$ propagates a fault effect and $d$ is the sequential depth of $z$ in $S$.

*Proof:* Since $t$ detects $f_j$, the value of $x_j$ in $t$ must be $\bar{v}$. Let $F(x_1, x_2, \cdots, x_n, X)$ be a function of $z$ in $C^*(S)$, where $X$ is a list of primary inputs other than $x_1, x_2, \cdots, x_n$. Without loss of the generality, we assume that $t$ propagates a value $D$ to $z$ in $C^*(S)$. As a result, the following holds.

$$\begin{aligned} F(t) &= 1 \\ F(t[x_j := v]) &= 0 \end{aligned}$$

Let $F^*(T, \tau)$ denote the value of $z$ in a time frame $\tau$ on applying an input sequence $T$ to $S$. Since $S$ is an internally balanced structure, $F^*(T, d) = F(T_c(T, S, z, d))$ holds. Let $F_f^*(T, d)$ denote the value of $z$ in a time frame $d$ on applying an input sequence $T$ to $S$ with a fault $f$.

(1) Case of $F(t) \neq F(t[x_1 := v, \cdots, x_n := v])$: Let $T$ be any sequence satisfying $t = T_c(T, S, z, d)$. In this case the following holds.

$$\begin{aligned} F^*(T, d) &= F(T_c(T, S, z, d)) \\ &= F(t) \\ F_f^*(T, d) &= F(t[x_1 := v, \cdots, x_n := v]) \\ &\neq F(t) \end{aligned}$$

Therefore, $f$ can be detected by any $T$.

(2) Case of $F(t) = F(t[x_1 := v, \cdots, x_n := v])$: Let $T'$ be any sequence satisfying $t[x_j := v] = T_c(T', S, z, d)$. In this case the following holds.

$$\begin{aligned} F^*(T', d) &= F(t[x_j := v]) = 0 \\ F_f^*(T', d) &= F(t[x_1 := v, \cdots, x_n := v]) \\ &= F(t) = 1 \end{aligned}$$

Therefore, $f$ can be detected by any $T'$. ■

Let $\mathcal{T}_{S,x,v}$ denote a set of test sequences (or test patterns) that detect a stuck-at-$v$ on a line $x$ in $S$. Assume that a primary input $x$ is separated into primary inputs $x_1, x_2, \cdots, x_n$ in $C^*(S)$. Theorem 2 implies that $\bigcup_{1 \leq j \leq n} \mathcal{T}_{C^*(S),x_j,v} \neq \emptyset \Rightarrow \mathcal{T}_{S,x,v} \neq \emptyset$ holds. We now show $\bigcup_{1 \leq j \leq n} \mathcal{T}_{C^*(S),x_j,v} \neq \emptyset \Leftarrow \mathcal{T}_{S,x,v} \neq \emptyset$.

**Theorem 3** Let $S$ be a circuit with an internally balanced structure, where a primary input $x$ is separated into $x_1, x_2, \cdots, x_n$ in $C^*(S)$. Then, $\bigcup_{1 \leq j \leq n} \mathcal{T}_{C^*(S),x_j,v} = \emptyset \Rightarrow \mathcal{T}_{S,x,v} = \emptyset$ holds.

*Proof:* We prove the theorem by contradiction. Assume $\bigcup_{1 \leq j \leq n} \mathcal{T}_{C^*(S),x_j,v} = \emptyset$ but $\mathcal{T}_{S,x,v} \neq \emptyset$. Let $T$ be a test sequence that detects a stuck-at-$v$ fault $f$ on $x$ in $S$ where $T$ propagates an error to an output $z$ in a time frame $\tau$. Let $F$ be a function of $z$ in $C^*(S)$. Since any stuck-at-$v$ fault $f_j$ on $x_j$ is redundant, $F(t) = F(t[x_j := 0]) = F(t[x_j := 1]) = F(t[x_j := v])$ holds for any $x_j$ and any input pattern $t$.

Since the primary input $x$ in $S$ is separated into $x_1, \cdots, x_n$ in $C^*(S)$ and $T$ is a test sequence for $f$, $F(T_c(T, S, z, \tau)) \neq F(T_c(T, S, z, \tau)[x_1 := v, \cdots, x_n := v])$ holds. However, the following also holds.

$$\begin{aligned} & F(T_c(T, S, z, \tau)) \\ = \; & F(T_c(T, S, z, \tau)[x_1 := v]) \\ = \; & F(T_c(T, S, z, \tau)[x_1 := v, x_2 := v]) \\ \cdots \\ = \; & F(T_c(T, S, z, \tau)[x_1 := v, \cdots, x_n := v]) \end{aligned}$$

The contradiction occurs. ■

# 4 Conclusions

In this paper, we considered the test generation problem for a single stuck-at-$v$ fault on a separable primary input $x$ of a sequential circuit with an internally balanced structure. We first showed that test sequences corresponding to test patterns for single stuck-at-$v$ faults on its separated primary inputs $x_1, x_2, \cdots x_n$ cannot always detect the fault on $x$. However, we showed that a single stuck-at-$v$ fault on $x$ can be detected if one of the stuck-at-$v$ faults on the separated primary inputs can be detected, and presented how to find a test sequence for the fault on $x$ using a test pattern for any of the separated primary inputs. We also showed that if any single stuck-at-$v$ fault on the separated primary inputs is redundant then a single stuck-at-$v$ fault on $x$ is also redundant. As a result, the test generation problem for single faults on separable primary inputs in a sequential circuit with an internally balanced structure can be reduced to the test generation problem for single faults in a combinational circuit.

In [1], it is shown that the test generation problem for single faults on all lines except for the separable primary inputs of a sequential circuit with an internally balanced structure can be reduced to the test generation problem for single faults in a combinational circuit. As a result, the test generation problem for *all* single faults in a sequential circuit with an internally balanced structure is reduced to the test generation problem for single faults in a combinational circuit.

# References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