Graduate School of Science and Technology Master's Thesis Abstract

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Thesis title	HPQEA: A Scalable and High-Performance Quantum Emulator with High-Bandwidth Memory for Diverse Algorithm Support		

Abstract

Quantum computing has emerged as a potential approach to solving problems that are too complex or time-consuming for classical computers. Its possible applications are numerous, including optimization, data fitting, machine learning, quantum chemistry, and large-scale scientific modeling. As these application areas continue to expand, the demand for reliable, efficient development of quantum algorithms grows. However, currently available quantum computers have severe limitations, such as a small number of quantum bits (¥#qubits), high susceptibility to noise and decoherence, and strict environmental controls. Furthermore, access to practical quantum devices is limited and expensive, resulting in significant experimental latency. Such constraints limit the development of quantum algorithms, underscoring the critical importance of quantum emulation on classical platforms.

Quantum emulation is an effective means of testing, validating, and refining quantum algorithms before they are deployed on genuine quantum devices. However, mimicking quantum circuits, particularly through state-vector simulation, presents significant computational and memory problems. The exponential growth in data storage for an n-qubit system leads to a rapid increase in resource requirements. While high-performance Central Processing Units (CPUs) and Graphics Processing Units (GPUs) boost processing capability, they consume a lot of power and have limited scalability as ¥#qubits increase. Other emulation methodologies, such as tensor networks, stabilizer formalisms, and density-matrix algorithms, are efficient only for certain circuit types and thus have limited applicability. Additionally, FPGA-based emulation has recently acquired popularity due to its energy efficiency and fine-grained hardware-level parallelism. Nevertheless, most prior FPGA approaches are limited to specific algorithm types, use limited memory structures, or struggle to scale up to high ¥#qubits systems.

To address these challenges, this thesis introduces the High-Performance Quantum Emulation Accelerator (HPQEA), a scalable, resource-efficient FPGA-based architecture that supports general quantum circuits through a state-vector-based emulation framework. HPQEA provides three significant architectural advances. First, a dual Processing Element Array (PEA) enables highly parallel single-qubit computations while reducing data dependency conflicts. Second, by reorganizing the scheduling and data-movement pipelines, an efficient Controlled-NOT (CX) Swapper significantly minimizes the delay associated with two-qubit CX operations. Third, HPQEA uses High-Bandwidth Memory (HBM) to overcome on-chip memory constraints and provide large-scale volume storage with high data bandwidth. These key improvements enhance computing efficiency and expand the practical scalability of FPGA-based emulation. The proposed system is developed and tested using the AMD Alveo U280 Field Programmable Gate Array (FPGA) platform. HPQEA can emulate quantum circuits with up to 30 qubits, which significantly outperforms the scalability of previous FPGA-based emulators. Furthermore, HPQEA also surpasses software emulators such as Qiskit (IBM's quantum emulation library) in fidelity and mean-square error (MSE) across a variety of benchmark circuit types. Furthermore, HPQEA continually exceeds related FPGA-based works and achieves faster normalized gate speeds (NGS) than the NVIDIA A100 GPU for systems with up to 20 qubits while using less electricity.