Capacitive Neuromorphic Computation Employing Nonlinearity Correction Techniques

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Abstract:
Artificial neural networks (ANNs) have permeated virtually every scientific and technological domain requiring cognitive functionality, owing to their exceptional performance in tasks such as classification, generation, and regression. However, the prevailing technology stack—computing ANNs on graphics processing units (GPUs)—now demands enormous amounts of energy, raising concerns regarding its long-term sustainability.
As an alternative, spiking neural networks (SNNs) executed on neuromorphic systems have emerged as a promising technology stack, offering comparable performance with markedly lower power consumption. Motivated by the data-reuse capabilities of synaptic weights and the inherent parallelizability of synaptic operations in neural networks, as well as by the invention of novel memristive devices that emulate biological synapses by integrating memory and computation, research on analog neuromorphic systems based on memristor crossbar arrays has proliferated. However, memristive computation relies on Ohm's law—multiplying stored resistance values by applied voltages to produce currents—thus generating heat that constitutes a significant new source of energy expenditure.
In response, we propose a fusion of memory and computation in neuromorphic circuits that employs purely capacitive elements ("memcapacitors") or circuits devoid of direct current (DC) conduction paths. Unlike memristive computation, capacitive computation is immune to IR drop and sneak-path–induced errors; however, accurate readout of computational results currently depends on area- and energy-intensive operational amplifiers (op-amps). Eliminating op-amps introduces nonlinearities in the readout process, thereby necessitating techniques to compensate for such distortions. The contributions of this work are twofold: first, the design of an op-amp–free, capacitive neuromorphic circuit; and second, methods for nonlinearity compensation to achieve accurate computation using this circuit. The proposed compensation strategies include (i) circuit nonlinearity-aware training (ii) time-domain subtractive readout (iii) circuit-aware rounding,