A Non-scan DFT Method for RTL Circuits

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Outline

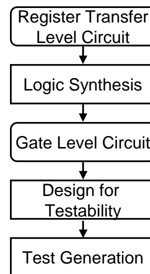
- Background
- Proposed method
- Experimental Results
- Conclusion

Importance of VLSI testing

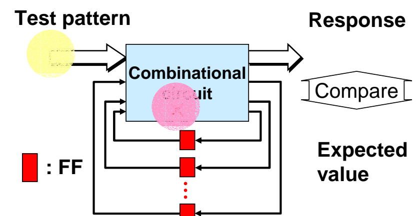
- **Ubiquitous computing**
  - Various tasks are performed anytime and anywhere

- **Testing of VLSI circuits**
  - Essential technology to realize dependable ubiquitous systems

VLSI Design Flow

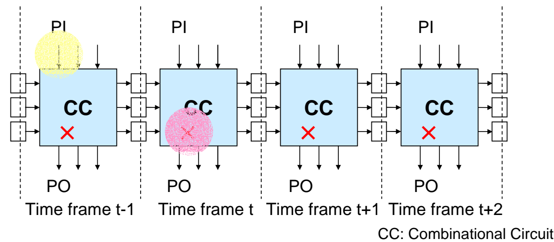


Traditional Design Flow



- **Test generation for combinational circuits**
  - Test generation is easy
  - 100% fault efficiency

Test Generation for Sequential Circuits



CC: Combinational Circuit

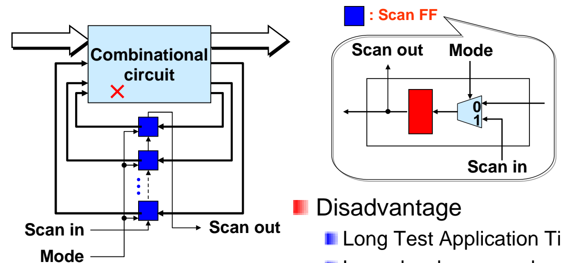
- Test generation for sequential circuits is too difficult
  - In the worst case, the number of time frames is 2^n

n: # of FFs

Design for testability (DFT) is important to ease test generation

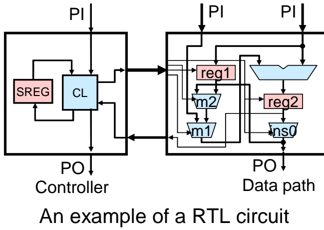
Practical DFT method: Full Scan Design

- Every FF is replaced by a scan FF

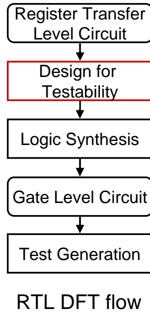


- Disadvantage
  - Long Test Application Time
  - Large hardware overhead
  - Can not test timing faults

Register Transfer Level (RTL) Circuit



An example of a RTL circuit



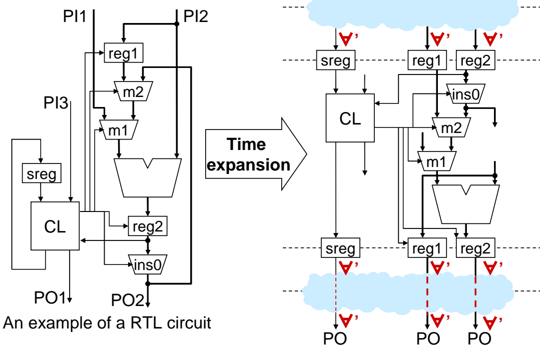
RTL DFT flow

- Related works of RTL DFT
  - Norwood et al. [1996]
  - Ohtake et al. [1998]
  - Wada et al. [1999]

Research Objectives

- Objectives
  - 100% fault efficiency (for single stuck-at-fault)
  - To reduce test application time
  - To reduce hardware overheads
  - To allow at-speed test
    - ⇒ not only stuck-at-faults but also timing faults
- Target Circuits
  - The whole RTL circuit
- Proposed method
  - Combinational test generation using *time expansion model*

Basic Idea of the proposed method

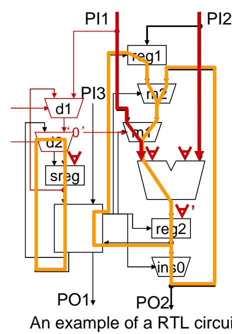


An example of a RTL circuit

∀': any value in normal operation

Difficult to realize in normal operation

DFT Method



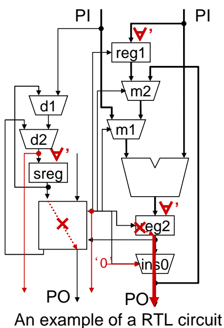
An example of a RTL circuit

- To set to ∀' to each registers
  - ∀ can be set to any loop independently
- Required DFT
  - Setting control signals
  - Adding control paths

∀ : any value

∀': any value in normal operation

DFT Method



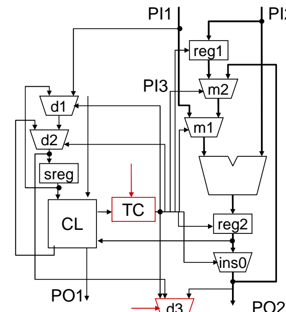
An example of a RTL circuit

- To observe from each registers
  - ∀' can be propagated from a loop to a PO
- Required DFT
  - Setting control signals
  - Adding observation paths

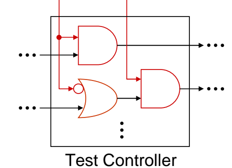
∀ : any value

∀': any value in normal operation

Test Controller (TC)



To realize DFT with low pin overhead



Test Controller

m1	m2	ins0	reg1	reg2	d1	d2
T	T	T	1	X	1	1
0	X	0	0	1	0	1
T	T	T	1	1	X	0
T	T	T	T	T	X	0

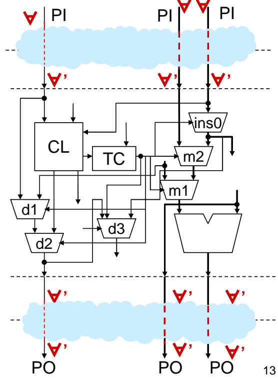
Output patterns of TC

T: output value of CL

X: don't care

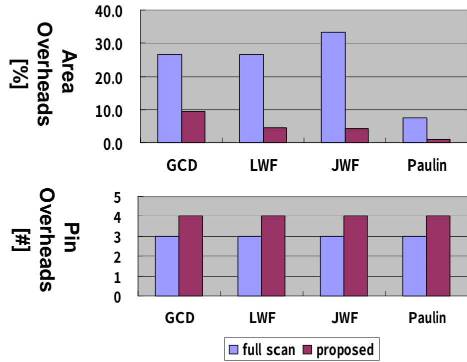
Test generation for proposed method

- Combinational test generation is applied to the time expansion model
  - # of time frames is less than fixed multiple of sequential depth from PI to PO
  - ⇒Test generation is easy

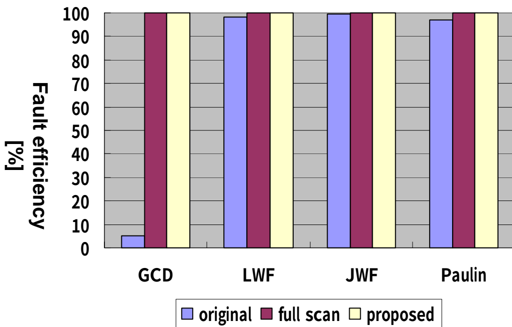


∀ : any value
∀': any value in normal operation

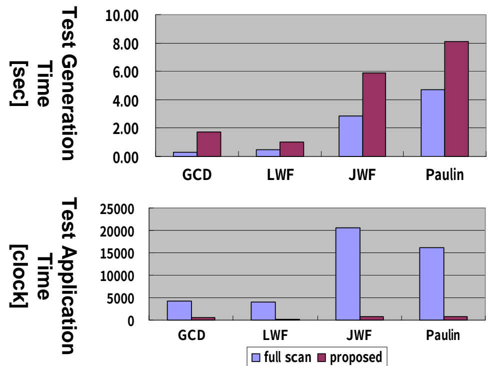
Experimental Results



Experimental Results



Experimental Results



Conclusion

- Proposed method
  - Combinational test generation applicable
- Advantages
  - 100% fault efficiency
  - Low hardware overheads compared with full scan method
  - Short test application time compared with full scan method
  - At speed test