Partially Strong Testability for RTL Circuits

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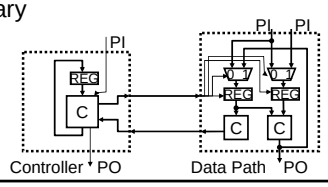
Outline

- Background
- Previous Research
  - Partially Strong Testability for Data Paths
- Present Research
  - Partially Strong Testability for the whole RTL Circuits
- Summary



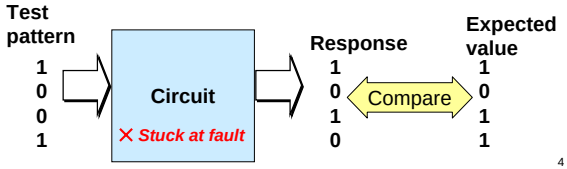
Importance of VLSI testing

- **Ubiquitous computing**
  - Various tasks are performed anytime and anywhere

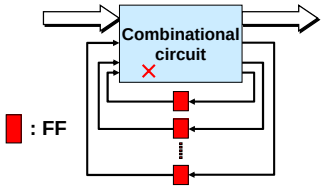
- **Testing of VLSI circuits**
  - Essential technology to realize dependable ubiquitous systems

VLSI Testing

- **VLSI Testing**
  - Check whether faults exist or not
- **Target fault**
  - Stuck at fault
- **Fault efficiency**
  - $\frac{\text{\# detected faults + identified \# redundant faults}}{\text{total \# faults}} \times 100$



Test Generation



test generation in practical time is too difficult

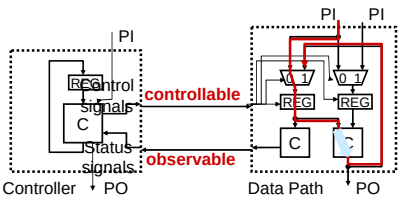
To ease the test generation

- **Design for testability (DFT)**
  - 100% fault efficiency
  - delay and area overhead as small as possible

Related work

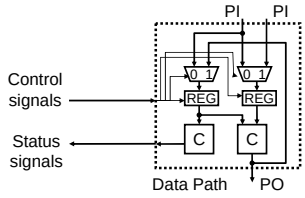
- DFT method based on Strongly Testability for RTL Data Paths [Wada at el. 1999]
  - Any hardware element is controllable along a simple path
  - Any hardware element is observable along a simple path

It is possible to test each hardware element

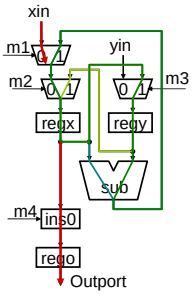


Our Previous work

- DFT method based on Partially Strong Testability for RTL Data Paths
  - To reduce the hardware overhead
    - Any loop is controllable along a simple path
    - Any loop is observable along a simple path

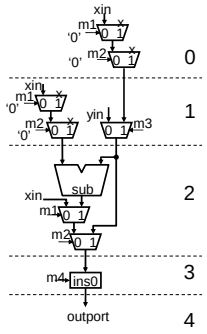


Partially Strongly Testability



An example of partially strongly testable data path

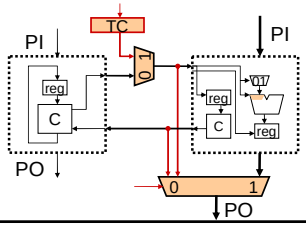
Time expansion



Time expansion model

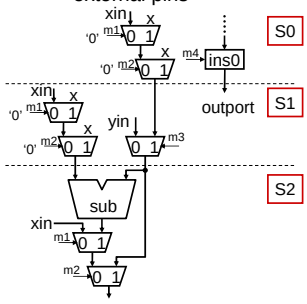
Remaining Problems

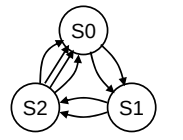
- Test Controller (TC)
  - To apply control signals with low pin overhead
- How large is the TC?



The generation of Test Controller

- Each frame of TEM is assigned to each state of TC
- The outputs of TC is controlled by states of TC and external pins





State transition of TC

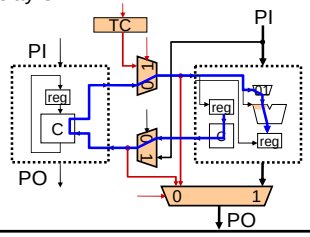
Experimental Results

The area overhead of TC

Benchmark Circuits	Circuit Area [unit]	TC area [unit]	Pin OH
GCD	2400	54	4
LWF	3412	62	6

Problems for the Method

- Problems
  - The testing of the controller
  - The area and pin OH of TC
  - The area OH to separate a data path and a controller
  - The delay OH

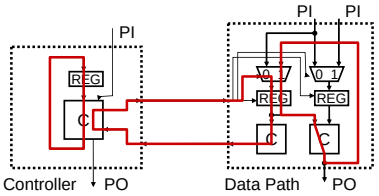


Research objectives

- Objectives
  - To reduce the hardware overhead of TC
  - To reduce the delay overhead
  - To test the controller
- Target Circuits
  - The whole RTL circuits
- Partially strong testability
  - The number of TEM is depended on the sequential depth of a simple path from PI to PO
  - Combinational ATPG is applicable

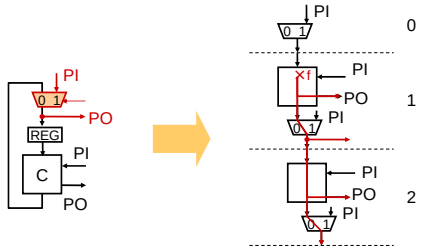
Partially Strong Testability for RTL Circuits

- Conditions for Partially Strong Testability
  - Any loop is controllable along a simple path
  - Any loop is observable along a simple path
- New problems
  - A circuit with two or more outputs
  - A loop with irregular bit width



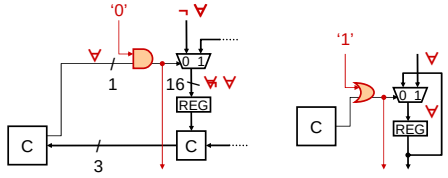
Design for Partially Strong Testability(1/2)

- Any loop which contains the hardware element with two or more output
  - Control path is added
  - Observation path is added



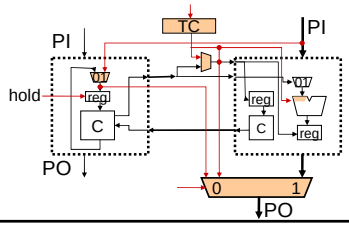
Design for Partially Strong Testability(2/2)

- A loop with irregular bit width
  - any value in normal operation can be justified to a loop
    - It is necessary to justify the any value which appear in the loop to the outside of the loop



Partially Strong Testability for RTL Circuits

- Every loop on the RTL circuit is controllable and observable
  - The control signals which TC controls are reduced
  - The signals which has the necessity for observation by PO are reduced



Summary

- Partially Strong Testability for RTL Circuits
  - Lower area and delay overheads compared to previous method
- Future works
  - Implementation of the DFT Algorithm and the TEM generation method
  - Experiments