Acceleration of Test Generation for Sequential Circuits Using Knowledge Obtained from Synthesis for Testability

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Outline
- Background
- Our proposed methods
  - Test generation method for sequential circuits
  - Synthesis for testability method
- Experimental results
- Conclusions

Importance of VLSI testing
- Ubiquitous computing
  - Various tasks are performed anytime and anywhere
- Testing of VLSI circuits
  - Essential technology to realize dependable ubiquitous systems

VLSI Testing
- VLSI Testing
  - Check whether faults exist or not
  - Fault efficiency
  - A rate scale which presents the quality of test patterns

Sequential Test Generation
- A sequential TG consists of three phases
  - Fault excitation
  - State justification
  - Error propagation

Time Frame Expansion
Related Works

- Previous works of sequential TG
  - Gate level
    - HITEC [Patel 91], TestGen [Synopsys], FASTEST [Kelsey 89], etc.
  - Utilizing knowledge extracted from FSMs
    - VERITAS [Cho '93]
      - State justification was accelerated
      - Error propagation was \textit{not} accelerated

I. Acceleration of fault excitation

- Searching for directly valid search space by using information of the valid states
- Pruning the search space of a test generation

II. Acceleration of state justification

- Justifying the excitation state by using state justification sequences extracted from a given FSM
- If an invalidation occurs, we try to propagate errors from the actual excitation frame

III. Acceleration of error propagation

- For fault-free circuit, a state distinguishing sequence for the pair of states of length \( \leq k \) is guaranteed
- For faulty circuit, if the sequence is valid for the pair of states \( (S_{t+1}, S_{t}) \), fast error propagation will be done

Our Proposed Methods

- Synthesis for Testability (SfT) method to synthesize a sequential circuit with three specific characteristics from an FSM
- TG method for the sequential circuit to utilize higher level knowledge of its features
  - Acceleration of fault excitation
  - Acceleration of state justification
  - Acceleration of error propagation

Experiment Environment

- We applied three methods to MCNC benchmark
  - TestGen + Original circuit
  - TestGen + SfT circuit
  - Proposed TG + SfT circuit
- Objective for comparison:
  - Test Generation Time (TGT)
  - Fault Efficiency (FE)
Experimental Results (TGT and FE)

<table>
<thead>
<tr>
<th>Circuits</th>
<th>TGT (sec)</th>
<th>FE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Original</td>
<td>SfT</td>
</tr>
<tr>
<td></td>
<td>circuit</td>
<td>circuit</td>
</tr>
<tr>
<td>bbara</td>
<td>10h</td>
<td>349.84</td>
</tr>
<tr>
<td>ext1</td>
<td>391.40</td>
<td>23841.81</td>
</tr>
<tr>
<td>keyb</td>
<td>1333.33</td>
<td>100</td>
</tr>
<tr>
<td>planet</td>
<td>69.66</td>
<td>102.62</td>
</tr>
<tr>
<td>s1</td>
<td>29918.96</td>
<td>7.70</td>
</tr>
<tr>
<td>s298</td>
<td>10h</td>
<td>10h</td>
</tr>
<tr>
<td>tma</td>
<td>692.22</td>
<td>223.86</td>
</tr>
<tr>
<td>tbk</td>
<td>10h</td>
<td>5.53</td>
</tr>
</tbody>
</table>

Conclusions

- We have proposed an efficient test generation method with an SfT method.
- Acceleration of each process by utilizing knowledge extracted from FSM during the SfT.
- Information of the valid states.
- State justification sequences.
- Length of state distinguishing sequences.
- Our proposed method can achieve 100% fault efficiency in shorter test generation time.
- This research was presented by the international conference WRTLT'05.

Future Work

- Study on Design for Testability of Instruction-Based Self-Test for pipelined microprocessors.
- It is difficult for Instruction-Based Self-Test to achieve 100% fault efficiency.
- We will be studying the design for testability method for instruction-based self-test which can achieve 100% fault efficiency.