COE Technical presentation

Design for Testability Based on Single-Port Change Delay Testing for Data Paths

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Outline

- Introduction to delay fault testing
  - Motivation
  - Delay fault testing
- Design for testability
  - Our previous work
  - Our proposed method
- Experimental result
  - Compare our method with previous one
- Conclusion

Motivation (1/2)

LSI is used in several equipment supporting ubiquitous network

- CPU, ASIC, Memory...

What is a good LSI ?

- High performance
- Small size
- Low price
- High reliability (correct behavior)

High quality and low cost testing is required

Motivation (2/2)

Progress in semiconductor technology

- The speed of VLSI circuits has increased

Require delay fault test to guarantee the timing correctness

Delay fault : the fault which prevents propagation of signals within the specified time

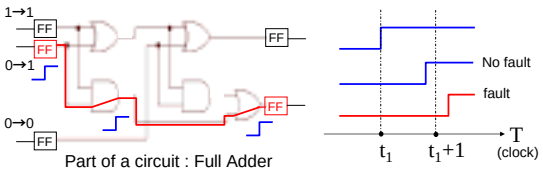
- Transition fault
- Segment delay fault
- Path delay fault (generally used model)

Path delay fault

Path delay fault

- Transitions launched at the starting point of a path cannot reach the ending point within the specified time

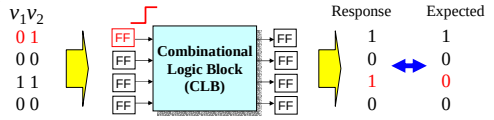
(Path: starts at a PI or a FF and ends at a PO or a FF)



Part of a circuit : Full Adder

Testing path delay faults

2 pattern test



v_1 : The pattern which initializes the circuit
v_2 : The pattern which launches and propagates the transition

Sequential circuit

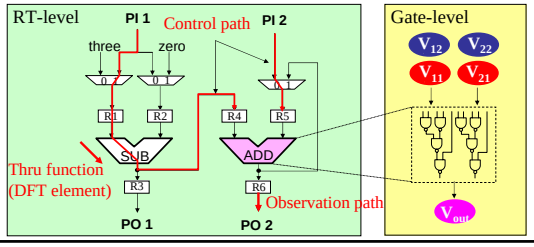
- Cannot apply any test patterns to FFs directly
- Sequence of test patterns should be applied to PIs

Design for Testability (DFT) have been researched widely

DFT based on hierarchical test [Amin *et al.*,2002]

Gate-level: Generating set of two-pattern tests for every combinational block (CLB)

RT-level : Applying the patterns to each CLB from PIs, and Observing the responses at POs



DFT based on hierarchical test [Amin *et al.*,2002]

The DFT method guarantees any two-pattern tests for every CLB by using control and observation paths

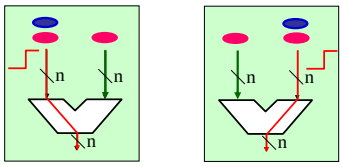
Advantages
- High fault coverage
- Short test application time
- Short test generation time

Disadvantages
- High area overhead
- Overtesting

} improved in our new method

Reduce area overhead

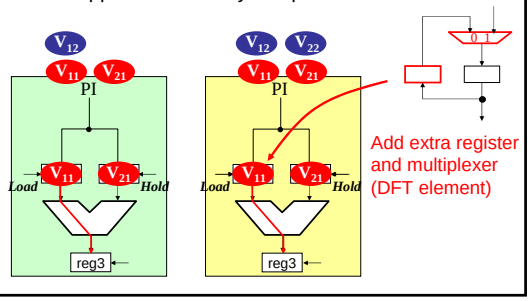
SPC two-pattern test
- First and second vectors are any values on one input port
- First vector is any value and second vector is the same as the first one on the other input port



SPC two-pattern test

What is the advantage of SPC

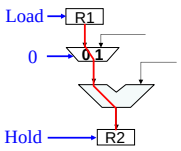
There are some cases where SPC two-pattern tests can be applied even if any two-patterns cannot



Reduce overtesting

- Extract Control-dependent Untestable Paths (CUPs) by analyzing control signals form a controller
- Except CUPs from target of testing

CUP
- The path never activated
- Transitions never propagated along the path within one clock period



Experiments

DFT for SPC two-pattern test *vs* DFT for any two-pattern test
- Hardware overhead
- Test application time

Table 1. Characteristics for benchmarks

Circuit	Bit width	PIs	POs	REGs	OPs	Area
Paulin	16	2	2	7	4	10,550
LWF	16	2	2	5	3	3,322
RISC	32	1	3	40	19	94,357
MPEG	8	7	16	241	157	77,554

RISC and MPEG are practical circuits designed by industry

Hardware overhead

Circuit	Bit width	SPC two-pat (%)	Any two-pat (%)
LWF	8	7.43	15.25
	16	6.38	13.99
Paulin	8	5.13	11.56
	16	3.30	7.43
RISC	32	0.64	1.99
MPEG	8	4.64	9.35

- Hardware overhead is reduced for all benchmarks

Test application time

Circuit	Bit width	SPC two-pat (cyc)	Any two-pat (cyc)	#CUPs
LWF	8	38,913	74,792	3 (19)
Paulin	8	785,136	1,645,335	11 (29)
RISC	32	$3T_{ALU}+2$	$4T_{ALU}+2$	512 (10,108)
MPEG	8	$186T_M+6111$	$186T_M+6049$	0 (651)

T_{ALU} : The number of test patterns for ALU
T_M : The number of test patterns for the main module of MPEG

Conclusion

Proposed the DFT method based on SPC two-pattern test
- Reduce hardware overhead
- Reduce test application time
- Reduce overtesting

Our future works
- A controller part
- Control signal lines and status signal lines