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The 5th COE Technical Presentation

A Design for 2-Pattern Testability of System-on-Chip Interconnects

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Outline

- Research Background
  - Testing of Interconnects
  - Design for 2-Pattern Testability
  - Related Works
- Serial 2-Pattern DFT
- Parallel 2-Pattern DFT
- Case Study
- Conclusion

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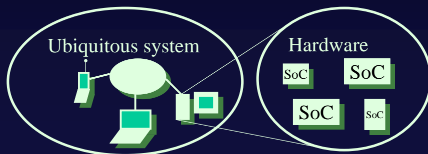
SoCs in Ubiquitous Systems

Many system-on-chips (SoCs) are used in ubiquitous system

SoCs need high reliability



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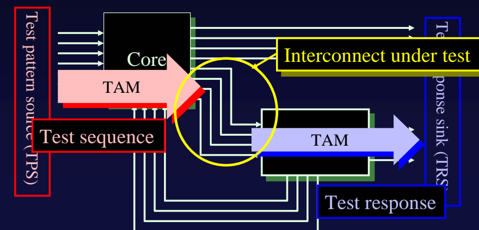
Testing of SoC

SoC: Cores and interconnects

Testing by test access mechanism (TAM)



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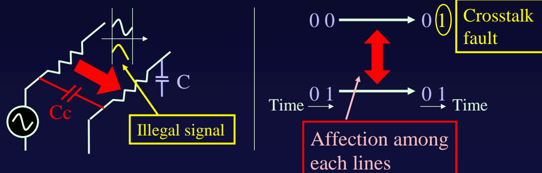
Testing of Interconnects

High integration of interconnects

Bit lines of interconnects affect each other

→ "Crosstalk"



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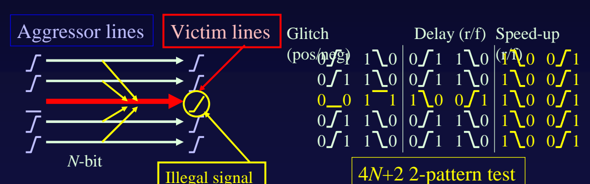
Maximal Aggressor (MA) Fault model (Cuviello et al., 1999)

1-bit victim line, and (N-1)-bit aggressor lines in N-bit interconnect

Victim line is affected by transition at all aggressor lines



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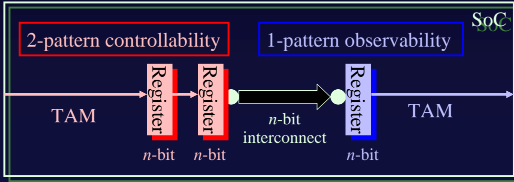
Design for 2-Pattern Testability (1/2)

2-pattern testability
- 2-pattern controllability: capability to apply arbitrary two patterns consecutively
- 1-pattern observability: capability to observe arbitrary one response



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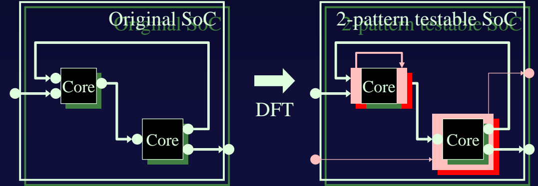
Design for 2-Pattern Testability (2/2)

Design for testability (DFT)
- Design a circuit to be tested easily (testability) by adding extra hardware



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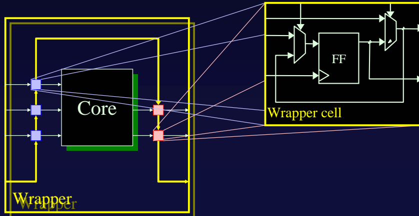
Related Works (1) - IEEE P1500 Wrappers

Architecture for SoC testing by IEEE
- INTEST: Test mode for cores
- EXTEST: Test mode for interconnects
- BYPASS: Transparent mode for test of other cores



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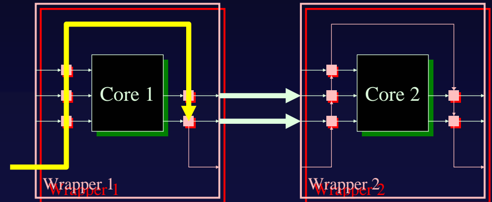
Testing of Interconnects by EXTEST

1. Scan test pattern into wrapper output cells
2. Apply test pattern to interconnects
3. Scan test response out from wrapper input cells



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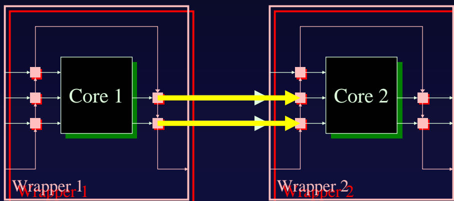

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Testing of Interconnects by EXTEST

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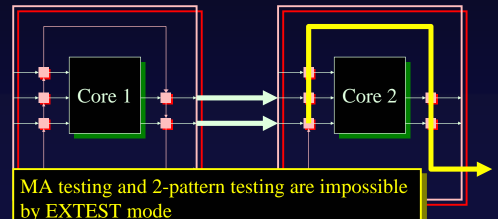


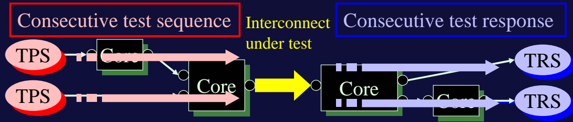
Related Works (2) - Design for Consecutive Testability (Yoneda et al., 2002)

Consecutive testability

- Consecutive controllability: capability to apply an arbitrary input sequence consecutively
- Consecutive observability: capability to observe an arbitrary response sequence consecutively

Testing of interconnects requires only two patterns

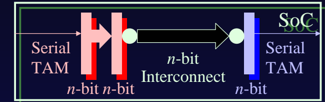
➡ Area overhead can be reduced



Objective of Our Work

We proposed two DFT methods for 2-pattern testability of interconnects

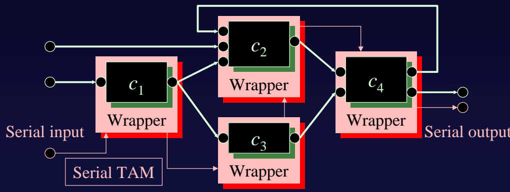
- Serial 2-pattern DFT - DFT with serial TAM



- Parallel 2-pattern DFT - DFT with parallel TAM

Serial 2-Pattern DFT (1/2)

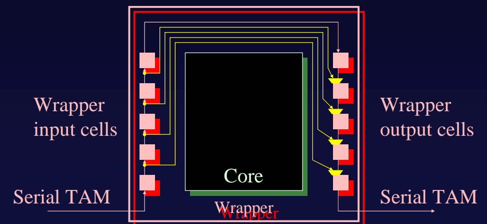
- Add wrappers to each core
- Add serial TAM through all wrappers



Serial 2-Pattern DFT (2/2)

- Add wrappers to each core
- Add serial TAM through all wrappers

To provide two patterns consecutively

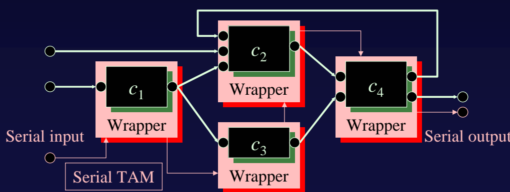


Serial 2-Pattern DFT Problem

Input: An SoC

Output: A serial TAM and wrappers that make all interconnects 2-pattern testable

Objective: Minimizing hardware overhead (No. of registers and MUXs, and area of additional lines)



Serial 2-Pattern DFT Algorithm

1. Design of wrapper for each core
2. Optimal design of a serial TAM that makes all interconnects 2-pattern testable

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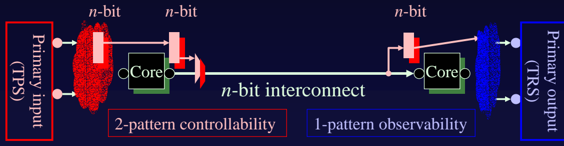
Parallel 2-Pattern DFT (1/3)

Design parallel TAM from TPS to TRS with registers, MUXs and signal lines



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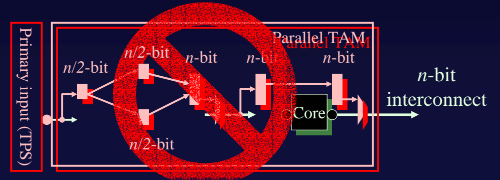
Parallel 2-Pattern DFT (2/3)

Design parallel TAM from TPS to TRS with registers, MUXs and signal lines

Parallel TAM internal:

Parallel TAM consists of extra hardware and existing interconnects

This parallel TAM is not 2-pattern testable



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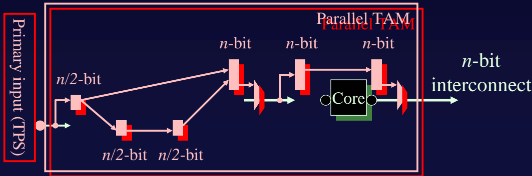
Parallel 2-Pattern DFT (3/3)

Design parallel TAM from TPS to TRS with registers, MUXs and signal lines

Parallel TAM internal:

Parallel TAM consists of extra hardware and existing interconnects

This parallel TAM is 2-pattern testable



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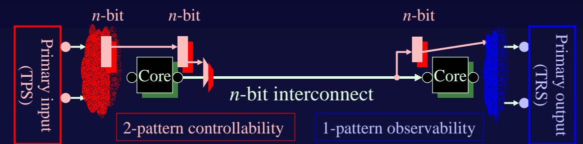
Parallel 2-Pattern DFT Problem

Input: An SoC

Output: A parallel TAM that makes all interconnects 2-pattern testable

Objective: Minimizing hardware overhead (No. of registers and MUXs, and area of additional lines)



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Parallel 2-Pattern DFT Algorithm

1. Optimal design of a parallel TAM that makes all interconnects 2-pattern controllable
2. Optimal augmentation of the parallel TAM that makes all interconnects 1-pattern observable

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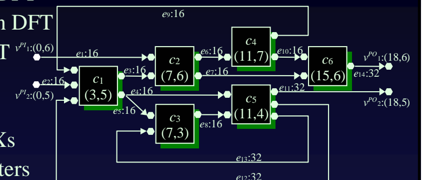
Case Study

We apply three DFTs to this sample SoC:

- Serial 2-pattern DFT
- Parallel 2-pattern DFT
- Consecutive DFT



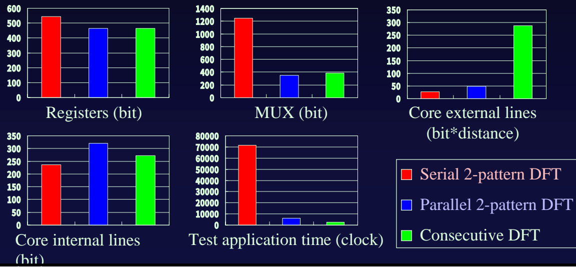
Evaluation:

- Number of MUXs
- Number of registers
- Area of additional signal lines
  - Core external lines: bit width * Manhattan distance
  - Core internal lines: bit width because distance is 0
- Test application time of MA test

Case Study Results

Serial 2-pattern DFT: Long test application time, large hardware area

Parallel 2-pattern DFT: Short test application time, small hardware area



Conclusion

We proposed designs for 2-pattern testability of interconnects

Serial 2-pattern DFT

- Large hardware and long test application time

Parallel 2-pattern DFT

- Small hardware and short test application time than both serial 2-pattern DFT and consecutive DFT

➡ Parallel 2-pattern DFT is effective method