Test Application Time Reduction with a Dynamic Reconfigurable Scan Tree Architecture

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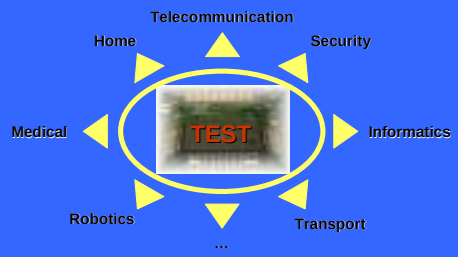
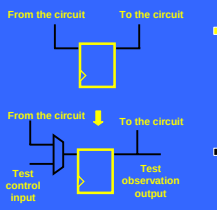
Motivation 1/2



Motivation 2/2

Scan Technique

- To reduce the test generation complexity
- To increase the test quality



- Efficient
- Reliable
- Proven
- Standardized

- Test power
- Test time

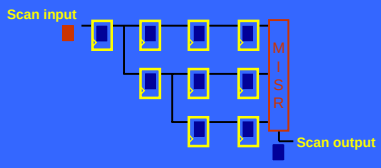
Outline

- Introduction
- Scan tree generation
  - Previous solution
  - New solution
- Experimental results
- Different optimizations
  - Fanout
  - Area-overhead
- Conclusion and future work

Introduction 1/3

- Scan tree architecture [Miyase03] [Yotsuyanagi03]

Shift time for 1 test pattern: 9



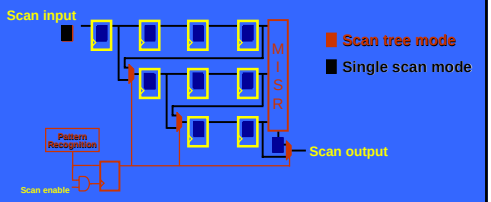
Shift time for 1 test pattern: 4

Introduction 2/3

- Scan tree architecture
  - Test time reduction
  - No additional test pin
  - High dependence between the scan tree design and the test sequence
  - Test sequence updating is no guaranty
  - It is not possible to provide a scan tree architecture in any case
- Dynamic reconfigurable scan tree architecture [Bonhomme04]

Introduction 3/3

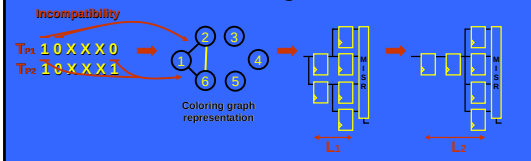
- The proposed architecture



- Which part of the test sequence for each mode?

Scan tree architecture generation 1/4

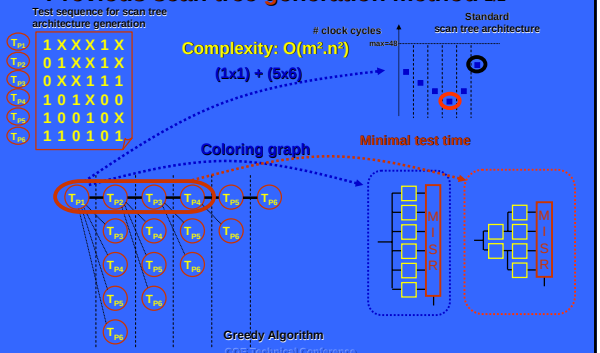
- Previous scan tree generation method 1/2



$L_2 > L_1$ TP_2 increases the constraint on the scan tree architecture

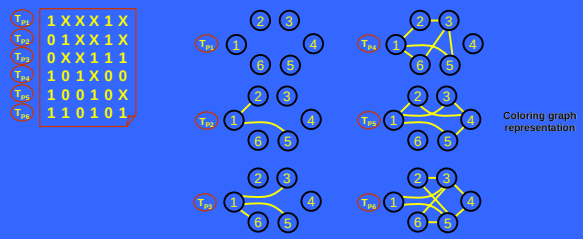
Scan tree architecture generation 2/4

- Previous scan tree generation method 2/2



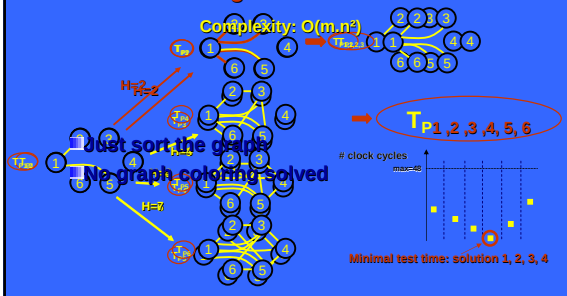
Scan tree architecture generation 3/4

- New scan tree generation method 1/2



Scan tree architecture generation 4/4

- New scan tree generation method 2/2



Experimental environment

Benchmark sets:	ISCAS'89 (scan version)
Test parameters:	Deterministic patterns TestGen by Synopsys
Simulation:	C code PIV 2.8GHz and 1Go

Experimental results 1/3

Benchmark set

	# FFs	# TPs (uncompacted)	# TPs (compacted)	FC
s5378	179	166	125	98,7%
s9234	211	341	228	93,16%
s13207	669	540	347	98,32%
s35932	1728	2835	X	X
s38584	1426	1275	X	X

Experimental results 2/3

Uncompacted test sequence

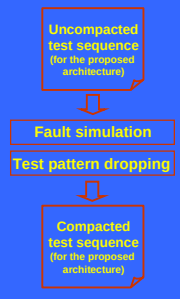
	Shift test time reduction*	Computation time (in seconds)	Shift test time reduction*	Computation time (in seconds)
s5378	72,70%	11	72,70%	5
s9234	58,30%	97	57,20%	29
s13207	87,80%	548	87,90%	222
s35932	99,51%	3940	99%	511
s38584	86,90%	14525	86,80%	399
	Previous technique		Proposed technique	

* Compared to the uncompacted test sequence applied in standard scan architecture

Experimental results 3/3

Compacted test sequence

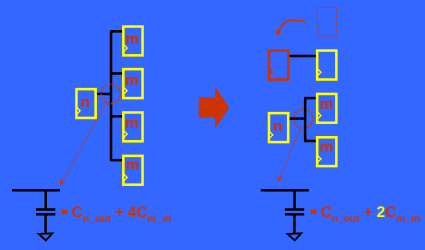
	Shift test time reduction*	Shift test time reduction*
s5378	68,21%	67,91%
s9234	46,25%	42,06%
s13207	83,99%	83,79%
s35932	90,05%	91,41%
s38584	X	X
	Previous technique	Proposed technique



* Compared to the compacted test sequence applied in standard scan architecture

Different optimizations 1/4

Fanout Optimization 1/2



Performance degradation

Different optimizations 2/4

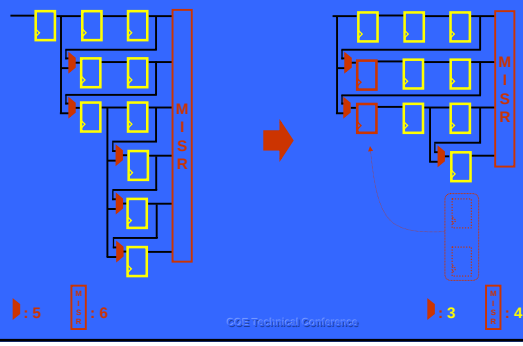
Fanout Optimization 2/2 – Fixed limitation: Fanout maximum =2

	Fanout average	Fanout maximum	Fanout average	Fanout maximum
s5378	1,42	12,5	1,13	1,93
s9234	1,08	4,77	1,05	2
s13207	1,3	5,4	1,21	2
s35932	6,29	27,11	1,2	2
s38584	1,1	2,12	1,05	2
	Before optimization		After optimization	

- Minimization of the delay-overhead
- Critical path can be safe
- No modification of the shift test time reduction

Different optimizations 3/4

Area-overhead Optimization 1/2



Different optimizations 4/4

- Area-overhead Optimization 2/2

	Before optimization		After optimization		Reduction	
	# Mux.	Size of the MISR	# Mux.	Size of the MISR	# Mux.	Size of the MISR
s5378	74	75	5	6	93,2%	92,0%
s9234	42	43	8	9	81,0%	79,1%
s13207	350	351	23	23	93,4%	93,4%
s35932	725	726	346	347	52,3%	52,2%
s38584	561	562	21	22	96,3%	96,1%

- No modification of the shift test time reduction

Conclusion

- Test time reduction up to 99%
- No additional test pins
- Flexibility
- Test sequence updating is possible
- Optimization Fanout / Area-overhead

Future work

- Include test power optimization
- Include design constraint: